

FIGURE 1.0

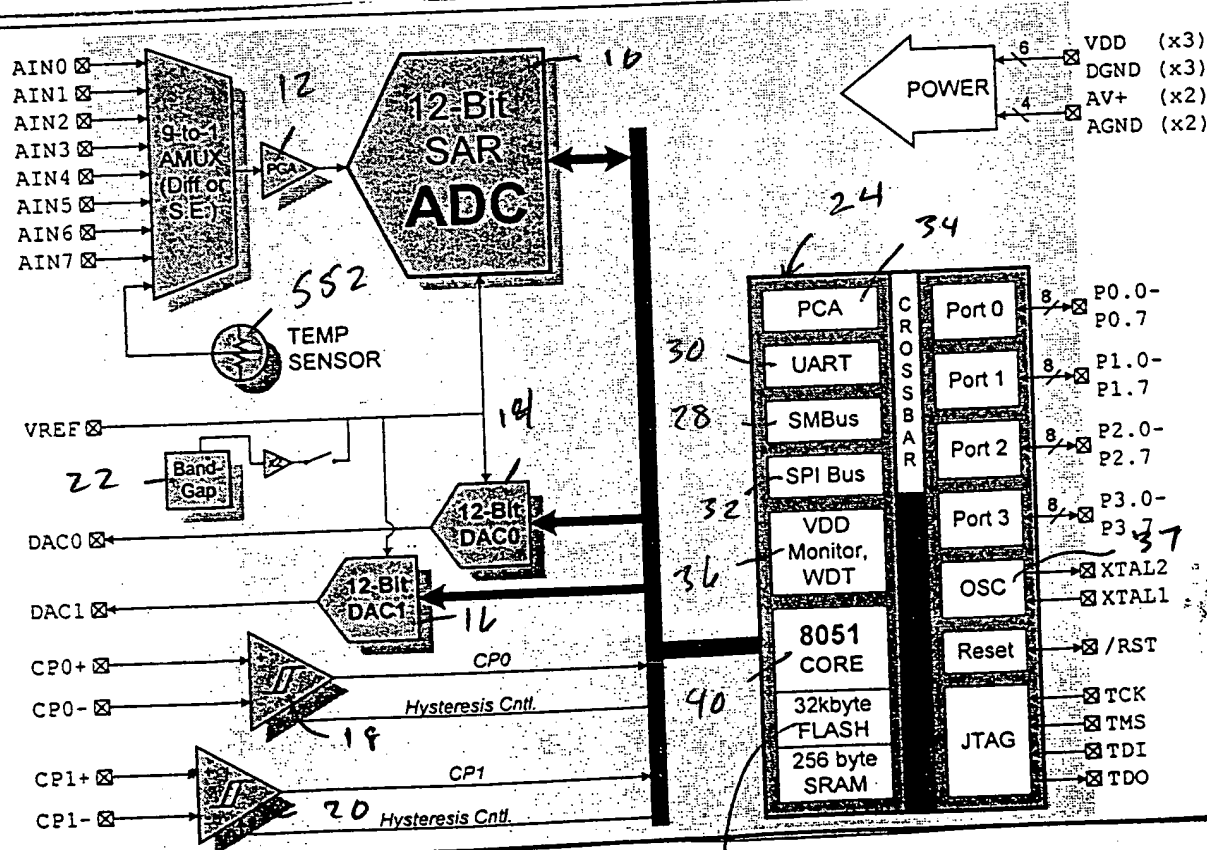
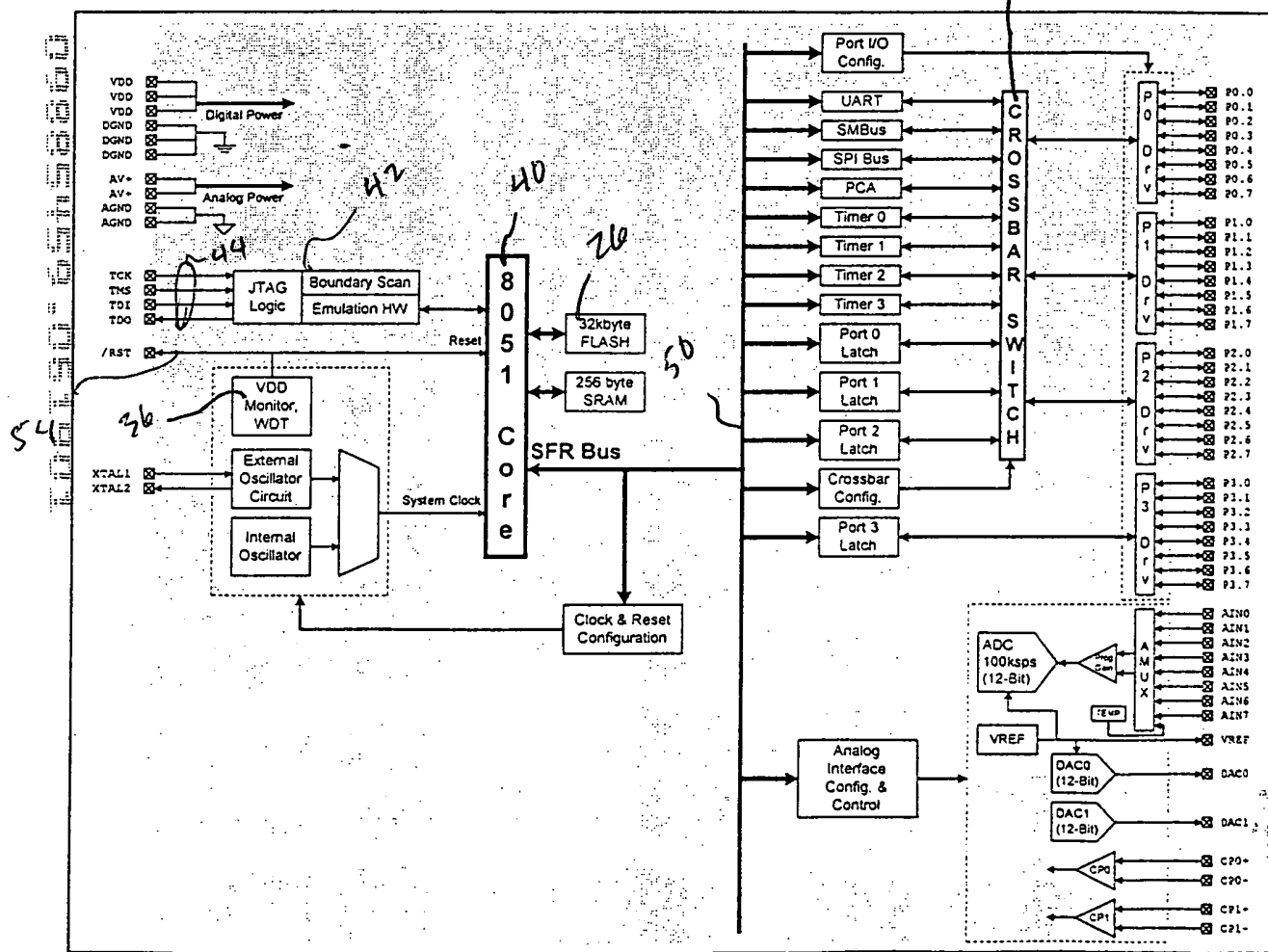
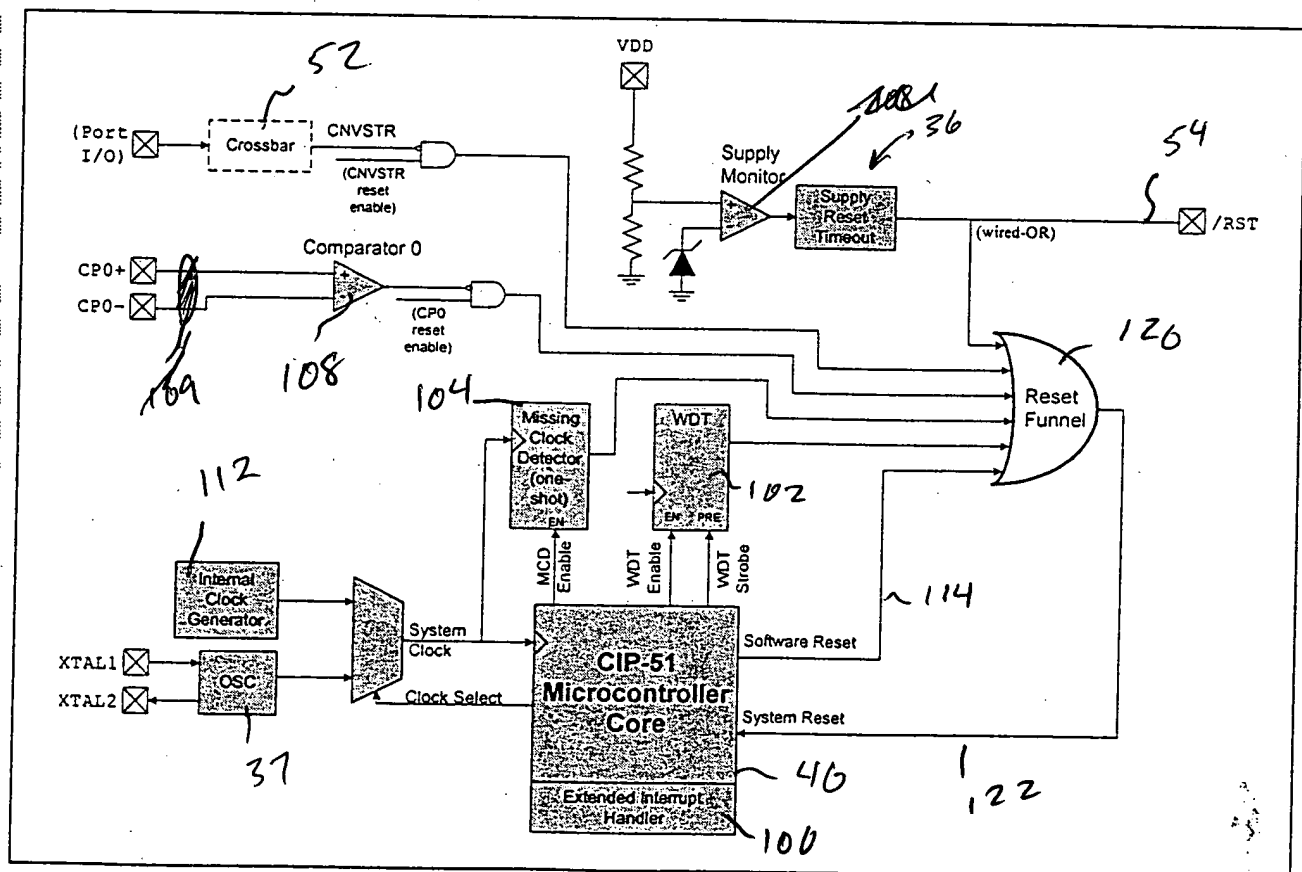


Figure 1.1. C8051F000 Block Diagram



43  
Figure 1.3. On-Board Clock and Reset



4  
4

Figure 1.4. On-Board Memory Map

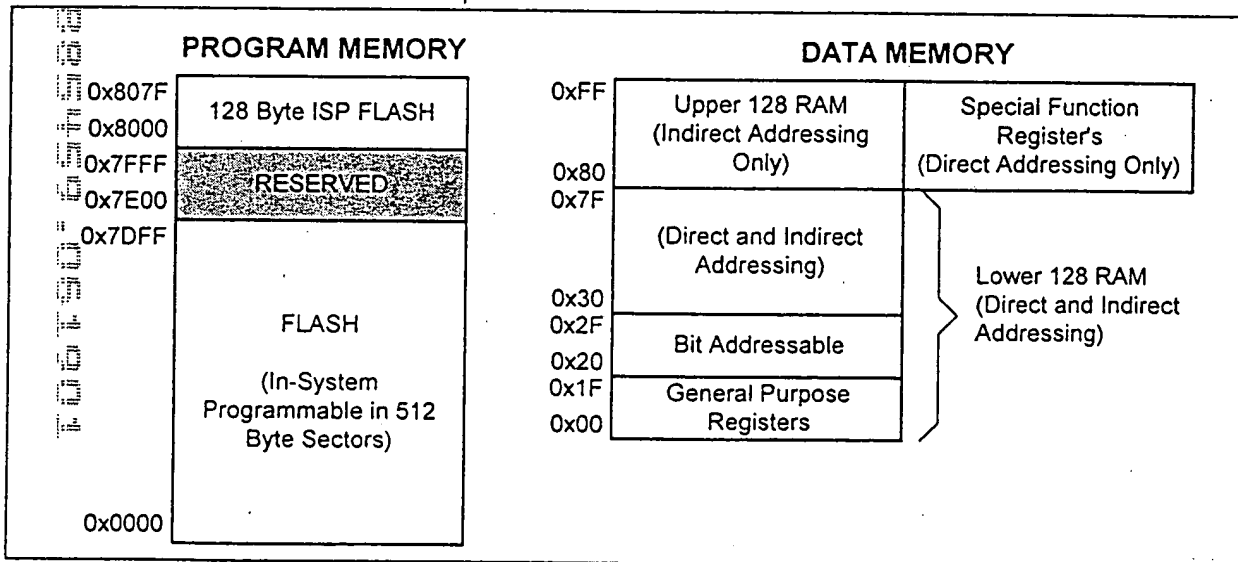


Figure 15. Emulation Diagram

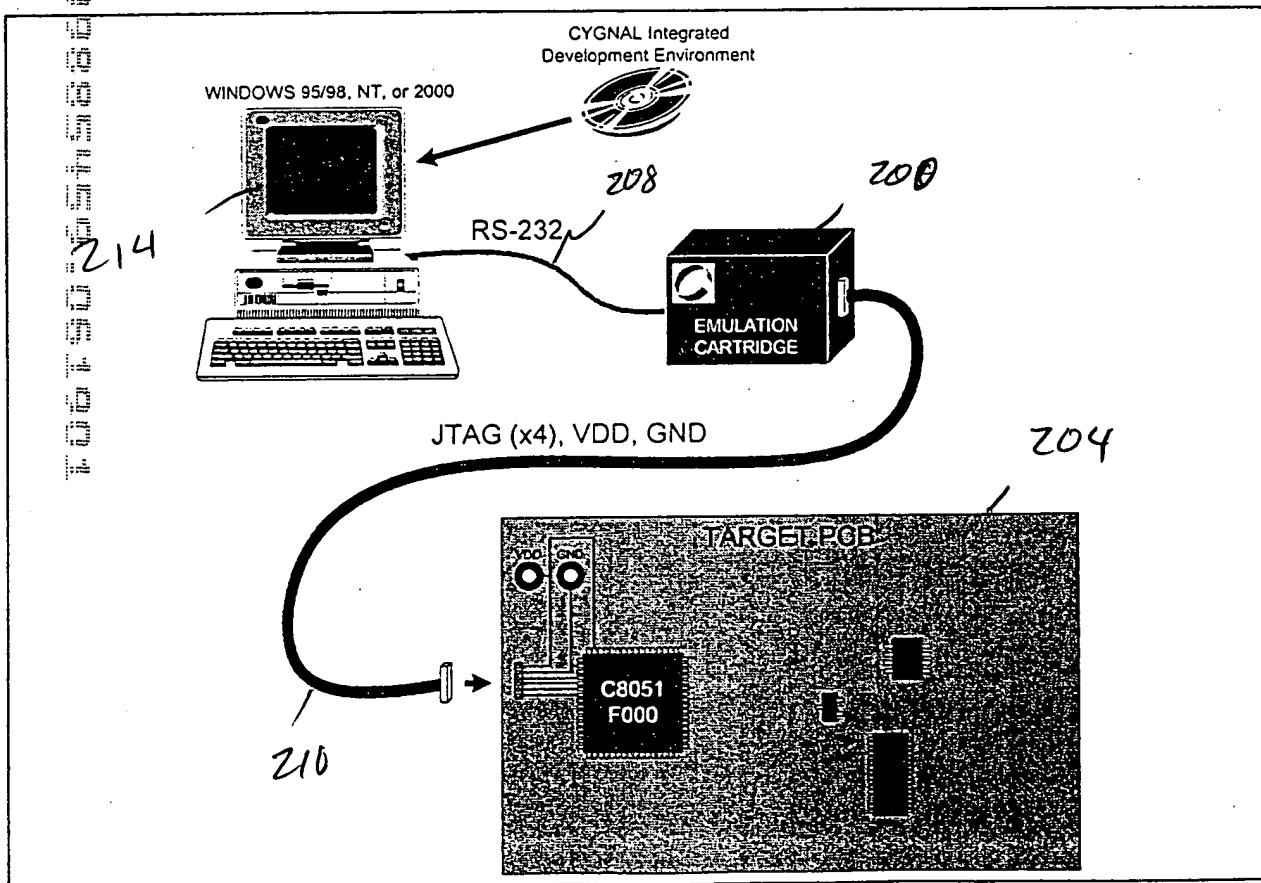
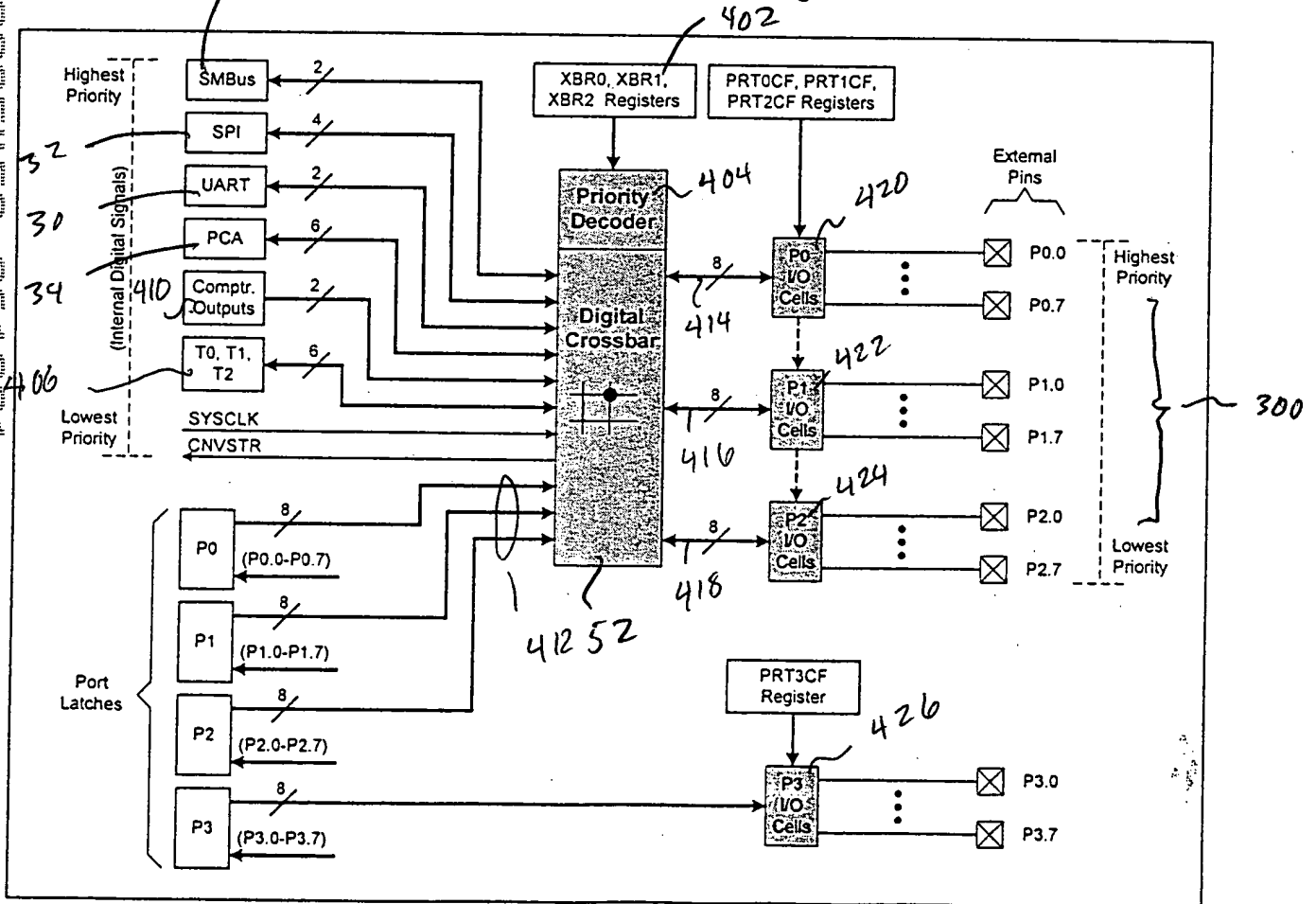
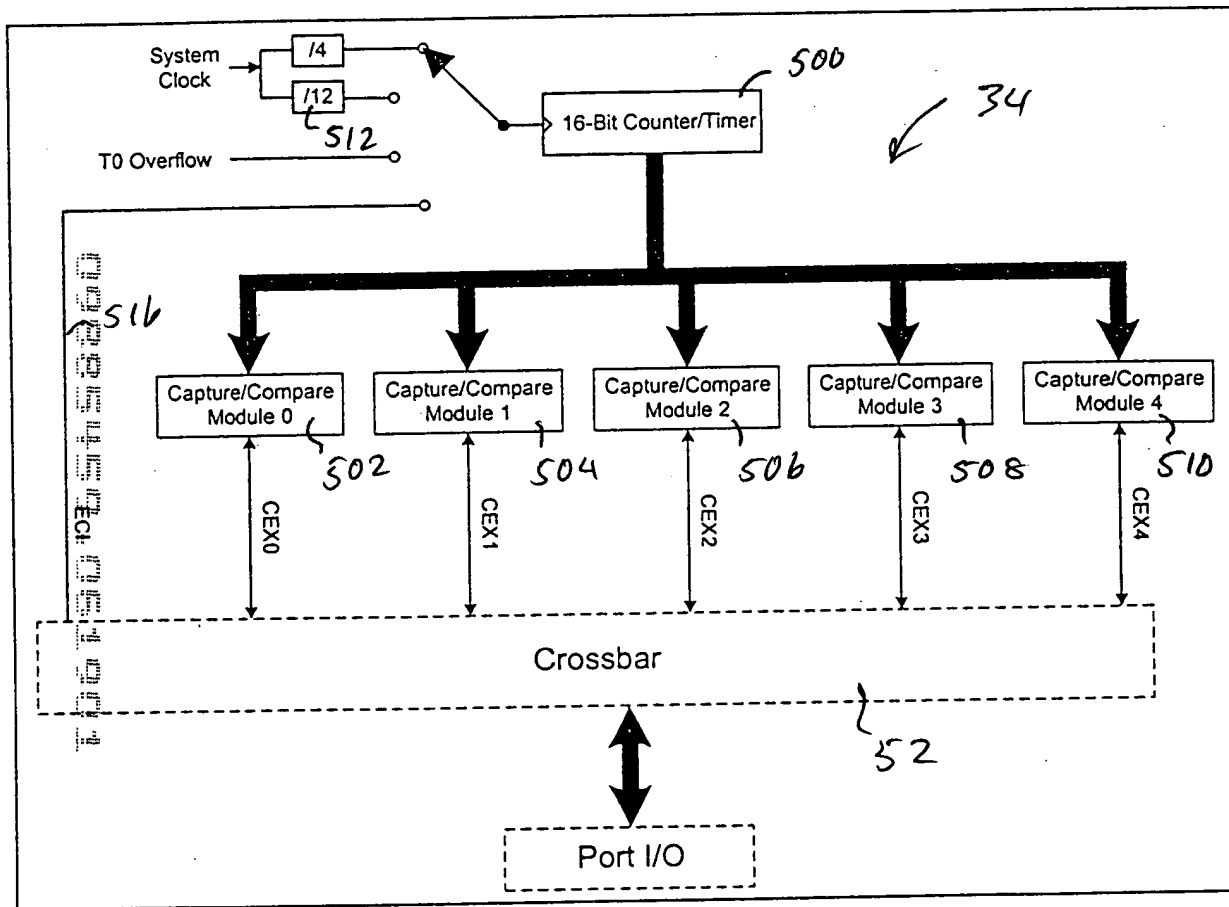


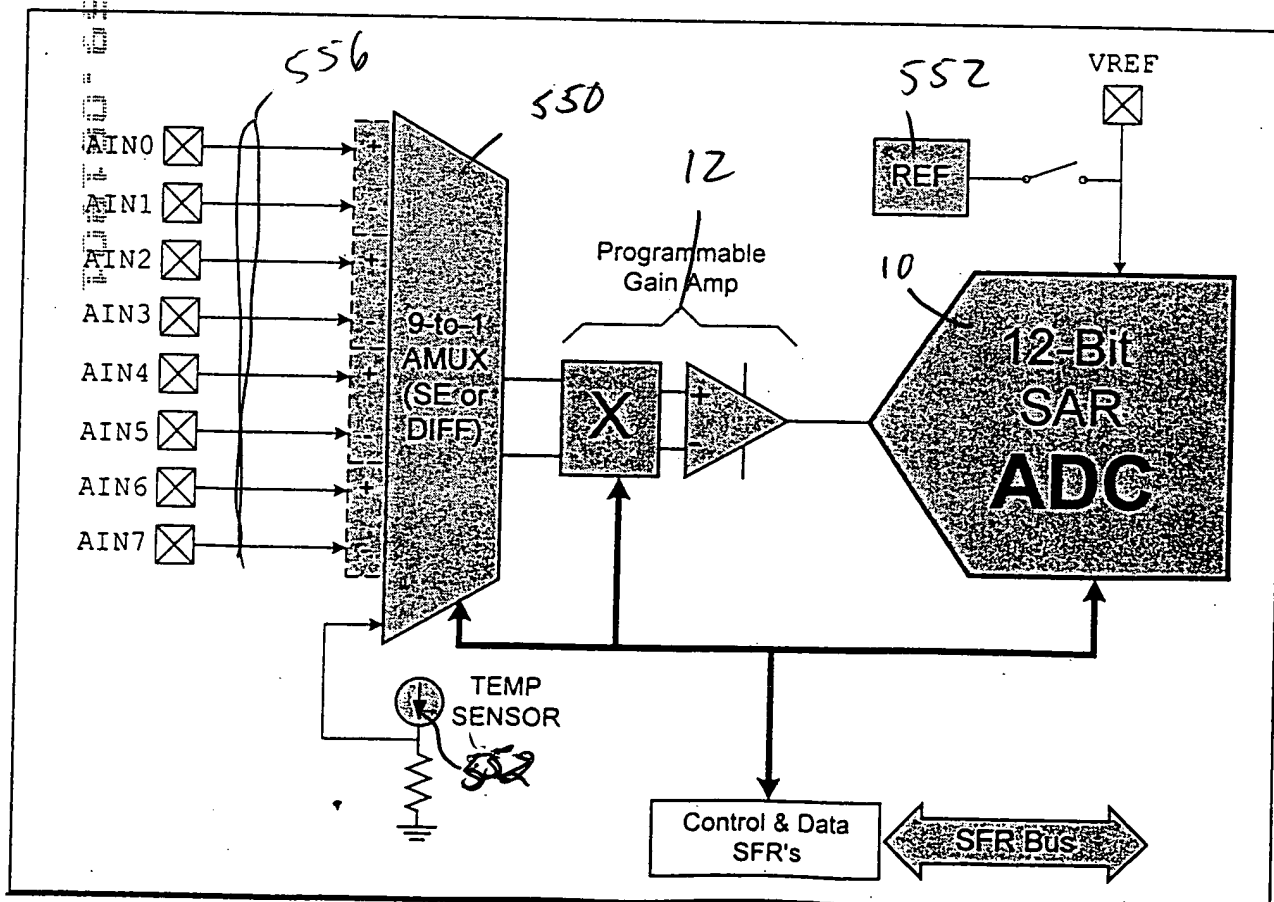
Figure 1.6. Digital Crossbar Diagram



87  
Figure 1.7. PCA Block Diagram

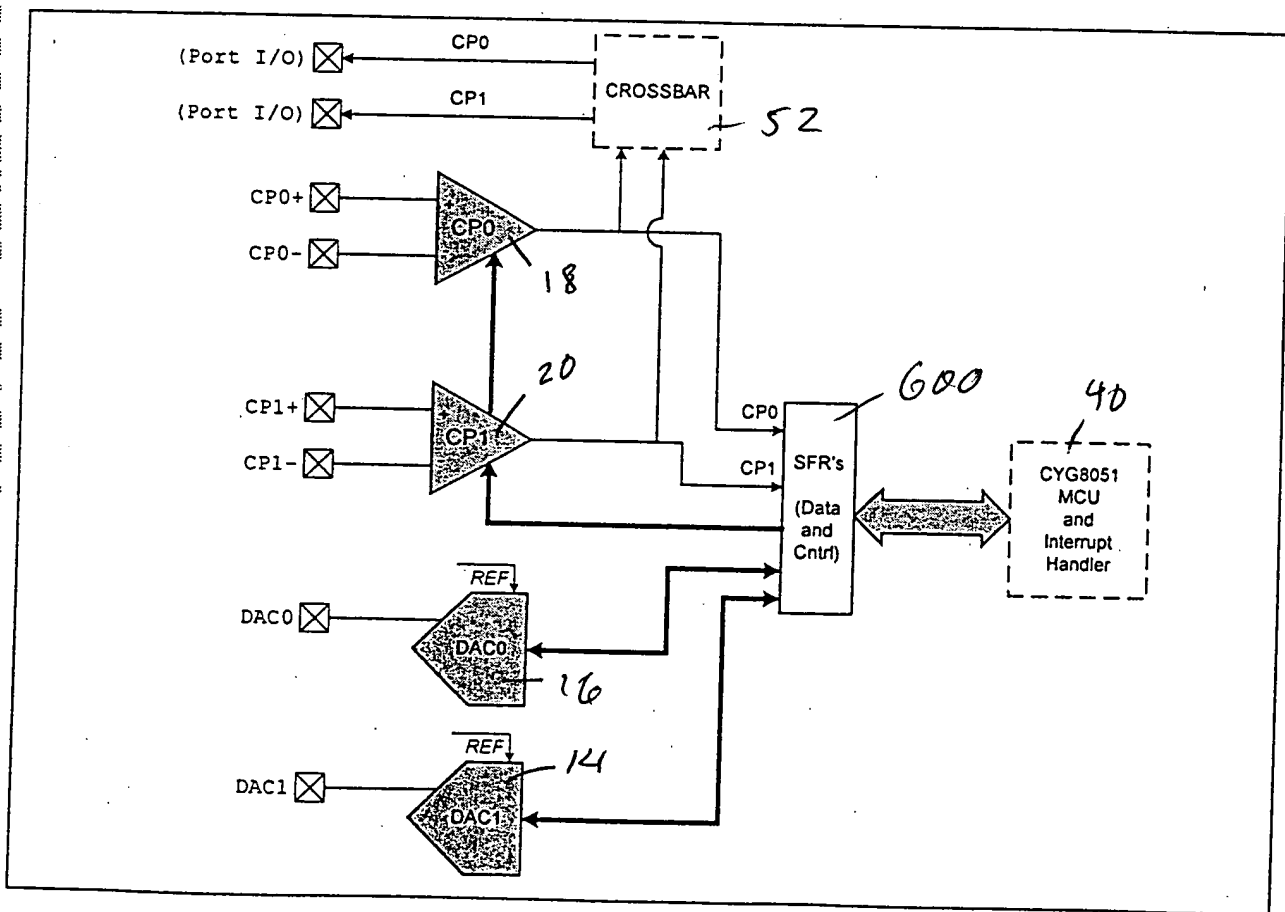


9108  
Figure 1.8. ADC Diagram





9  
~~18~~  
Figure 1.9. Comparator and DAC Diagram



26  
HB

[illegible]

Figure 5.2. ADC Track and Conversion Example Timing

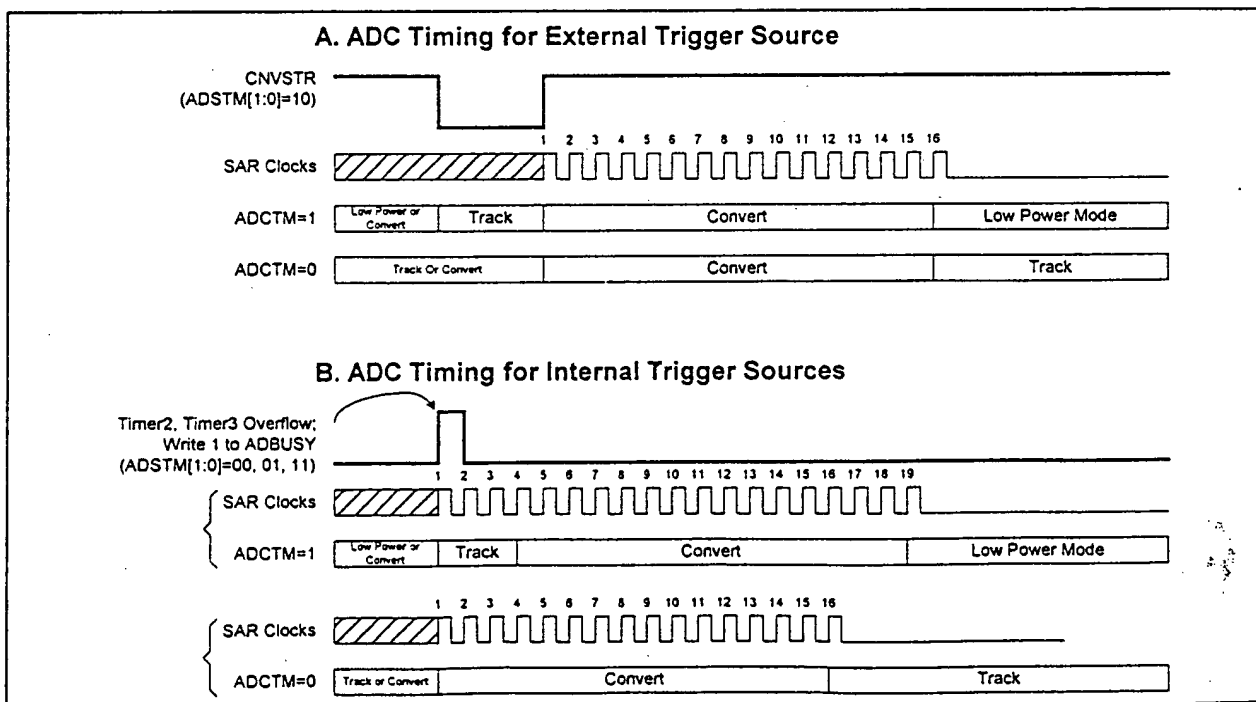
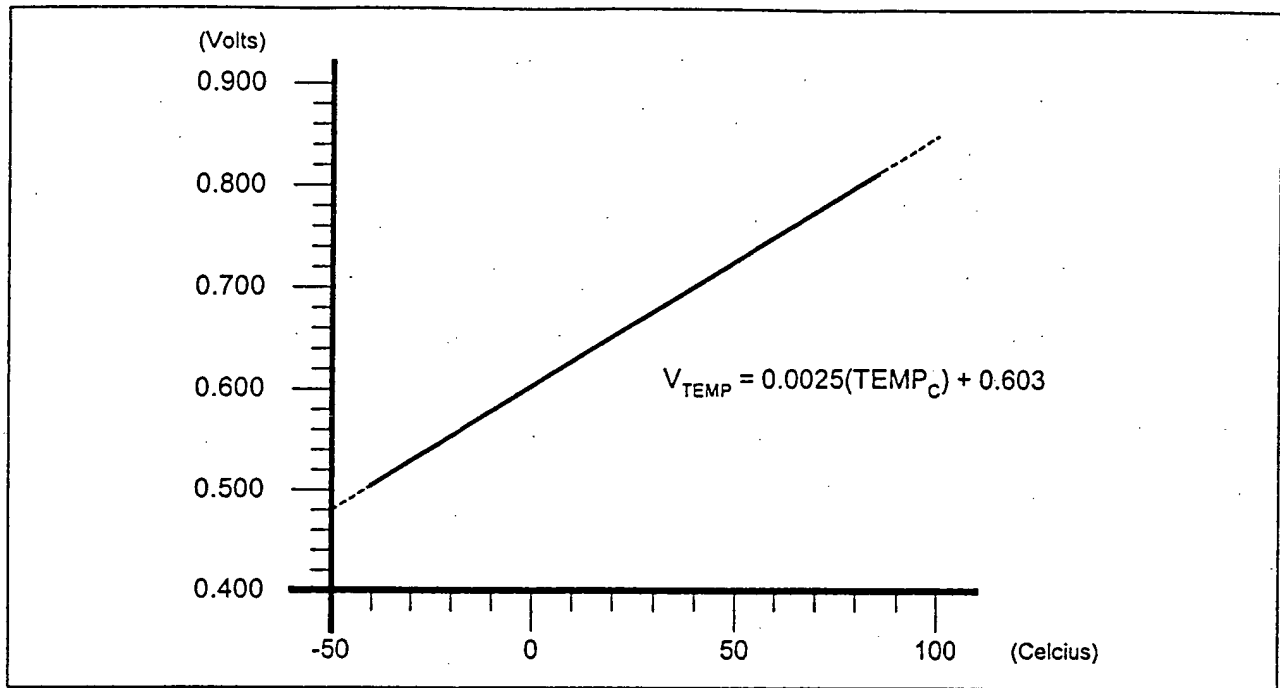


Figure 5.3. Temperature Sensor Transfer Function



T06T50 = 6345260

[illegible]

Input Voltage (AD0 - AGND)	ADC Data Word	
REF x (4095/4096)	0x0FFF	} ADWINT=1
	0x0201	
REF x (512/4096)	0x0200	ADC0GTH:ADC0GTL
	0x01FF	ADWINT not affected
	0x0101	
REF x (256/4096)	0x0100	ADC0LTH:ADC0LTL
	0x00FF	} ADWINT=1
0	0x0000	

**Given:**

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 0,  
ADC0LTH:ADC0LTL = 0x0100,  
ADC0GTH:ADC0GTL = 0x0200.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0100 or > 0x0200.

Input Voltage (AD0 - AD1)	ADC Data Word	
REF x (4095/4096)	0x07FF	} ADWINT=1
	0x0101	
REF x (256/4096)	0x0100	ADC0GTH:ADC0GTL
	0x00FF	ADWINT not affected
	0x0000	
REF x (-1/4096)	0xFFFF	ADC0LTH:ADC0LTL
	0xFFFE	} ADWINT=1
-REF	0xF800	

**Given:**

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 0,  
ADC0LTH:ADC0LTH = 0xFFFF,  
ADC0GTH:ADC0GTL = 0x0100.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0xFFFF or > 0x0100. (Two's Complement

Figure 5.15:

Window Interrupt Examples, Left

ified Data

Input Voltage (AD0 - AGND)	ADC Data Word	
REF x (4095/4096)	0xFFFF0	ADWINT not affected
	0x2010	
REF x (512/4096)	0x2000	ADWINT=1
	0x1FF0	
	0x1010	ADWINT=1
REF x (256/4096)	0x1000	
	0x0FF0	ADWINT not affected
0	0x0000	

Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,  
ADC0LTH:ADC0LTL = 0x2000,  
ADC0GTH:ADC0GTL = 0x1000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x2000 and > 0x1000.

Input Voltage (AD0 - AGND)	ADC Data Word	
REF x (4095/4096)	0xFFFF0	ADWINT=1
	0x2010	
REF x (512/4096)	0x2000	ADWINT not affected
	0x1FF0	
	0x1010	ADWINT=1
REF x (256/4096)	0x1000	
	0x0FF0	ADWINT=1
0	0x0000	

Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,  
ADC0LTH:ADC0LTL = 0x1000,  
ADC0GTH:ADC0GTL = 0x2000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x1000 or > 0x2000.

Input Voltage (AD0 - AD1)	ADC Data Word	
REF x (4095/4096)	0x7FF0	ADWINT not affected
	0x1010	
REF x (256/4096)	0x1000	ADWINT=1
	0x0FF0	
	0x0000	ADWINT=1
REF x (-1/4096)	0xFFFF0	
	0xFFE0	ADWINT not affected
-REF	0x8000	

Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 1,  
ADC0LTH:ADC0LTL = 0x1000,  
ADC0GTH:ADC0GTL = 0xFFFF0.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x1000 and > 0xFFFF0. (Two's Complement math.)

Input Voltage (AD0 - AD1)	ADC Data Word	
REF x (4095/4096)	0x7FF0	ADWINT=1
	0x1010	
REF x (256/4096)	0x1000	ADWINT not affected
	0x0FF0	
	0x0000	ADWINT=1
REF x (-1/4096)	0xFFFF0	
	0xFFE0	ADWINT=1
-REF	0x8000	

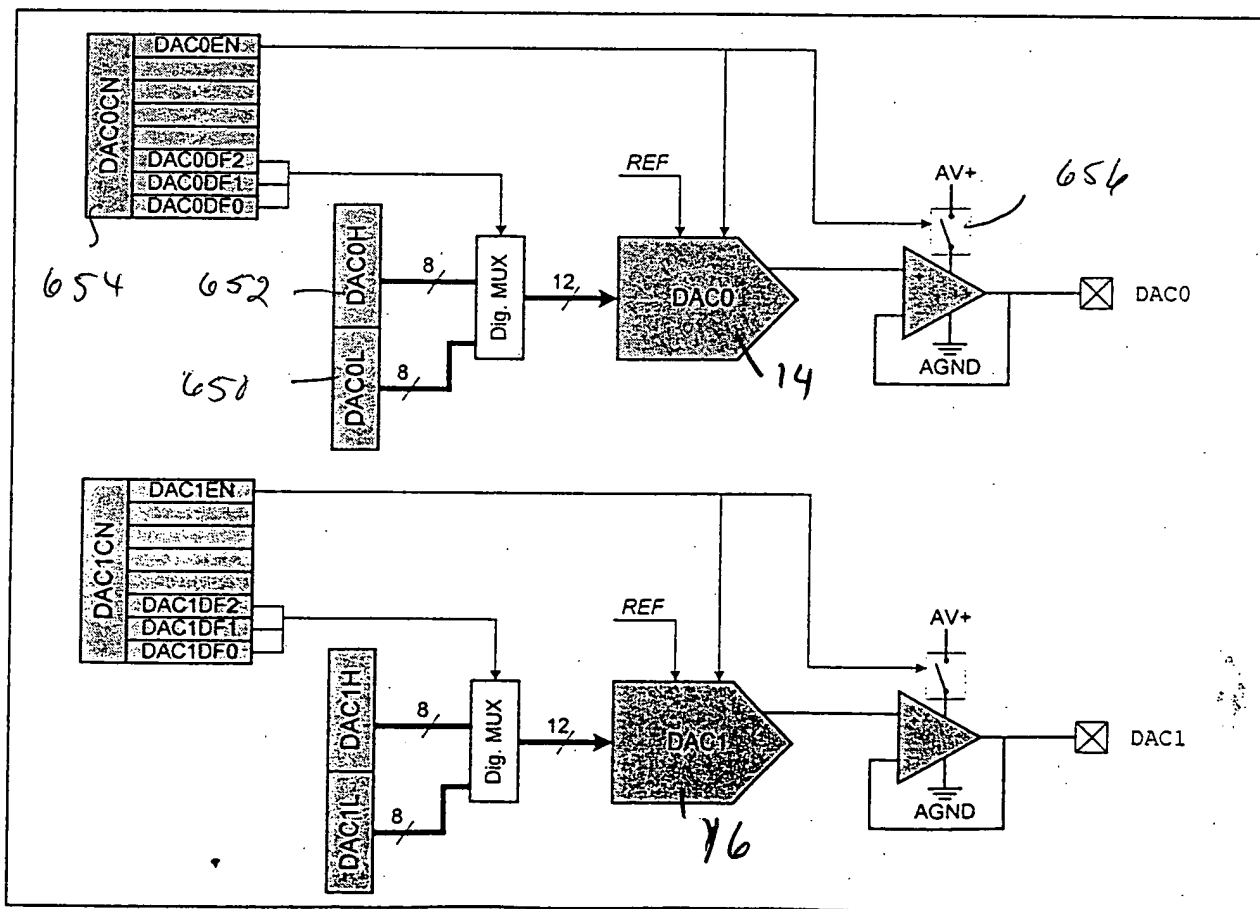
Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 1,  
ADC0LTH:ADC0LTH = 0xFFFF0,  
ADC0GTH:ADC0GTL = 0x1000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0xFFFF0 or > 0x1000. (Two's Complement math.)

are given in Table 0.1.

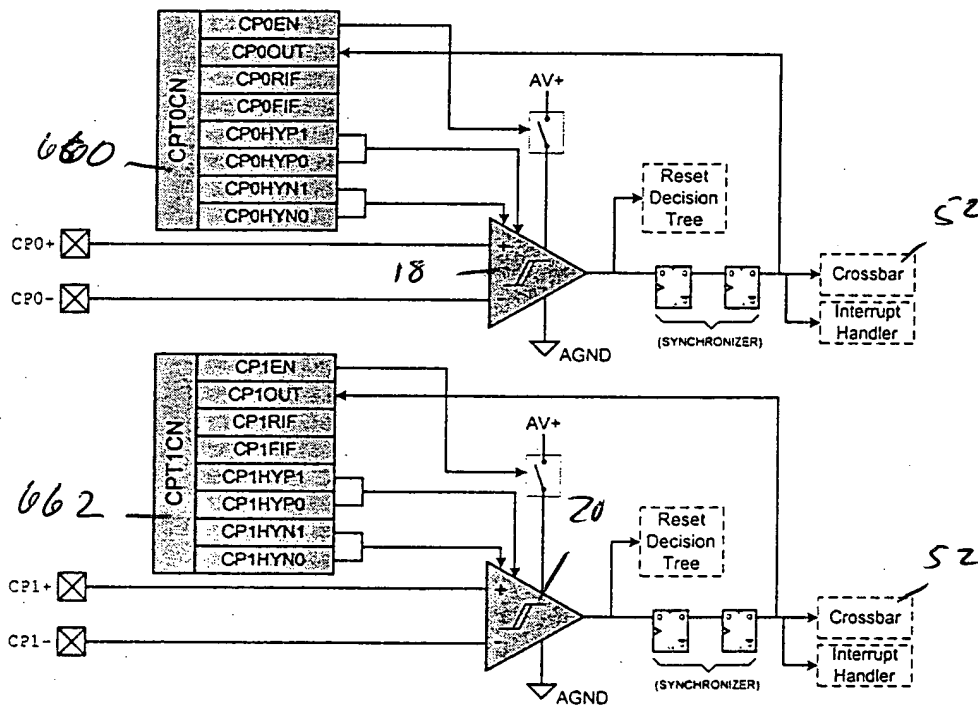
~~15~~ 15  
Figure 6.1. DAC Functional Block Diagram



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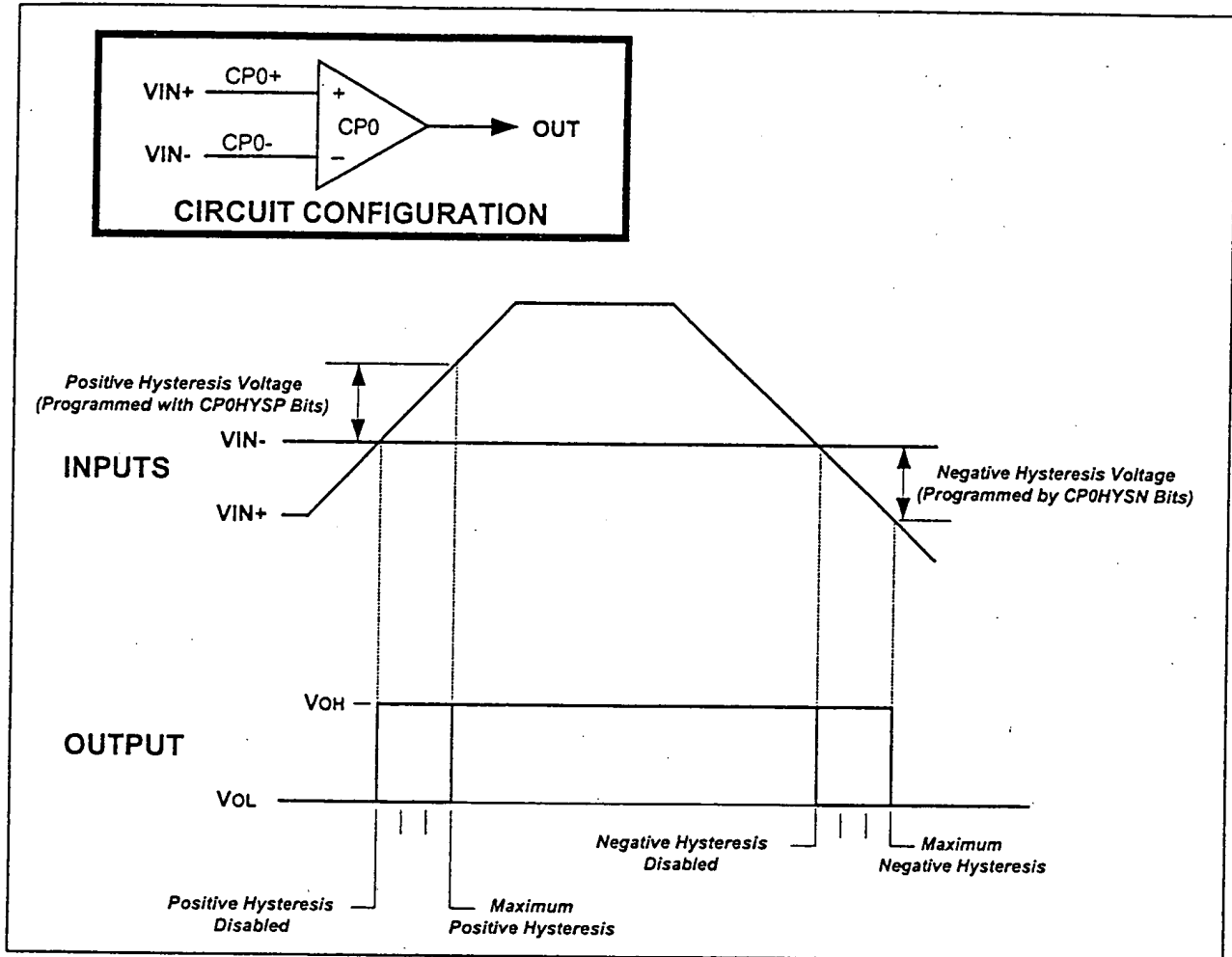
Figure 7.1. Comparator Functional Block Diagram





2017

Figure 7.2. Comparator Hysteresis Plot



21<sup>18</sup>

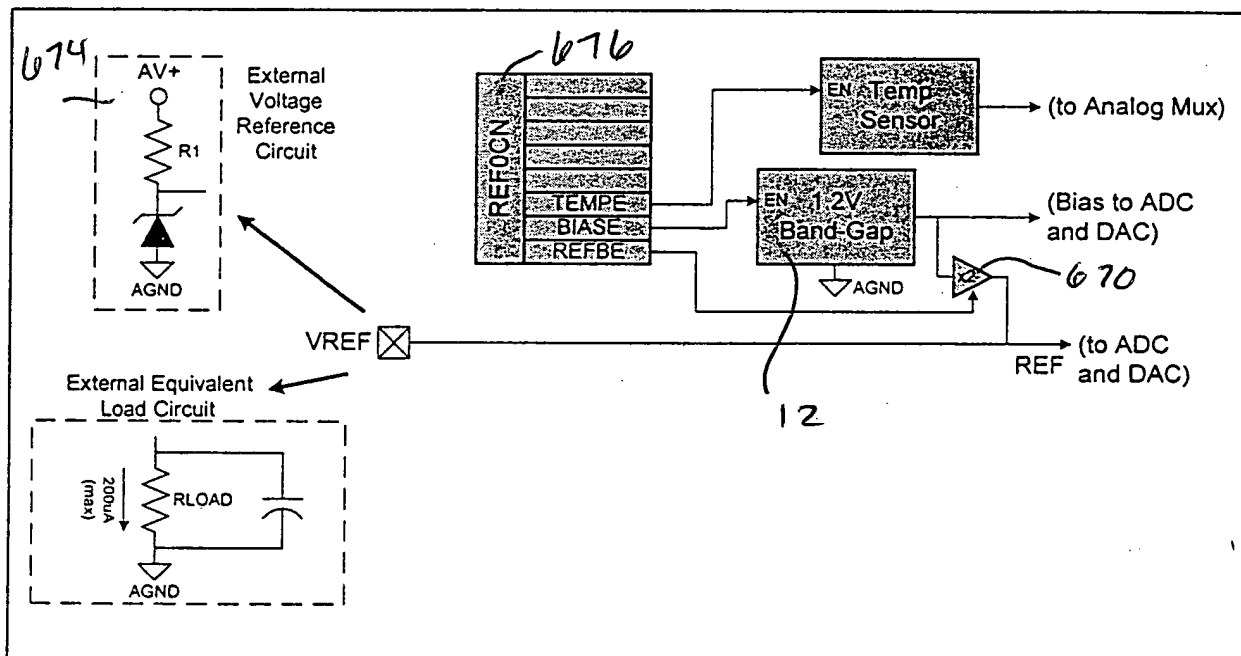


Figure 9.1. CIP-51 Block Diagram

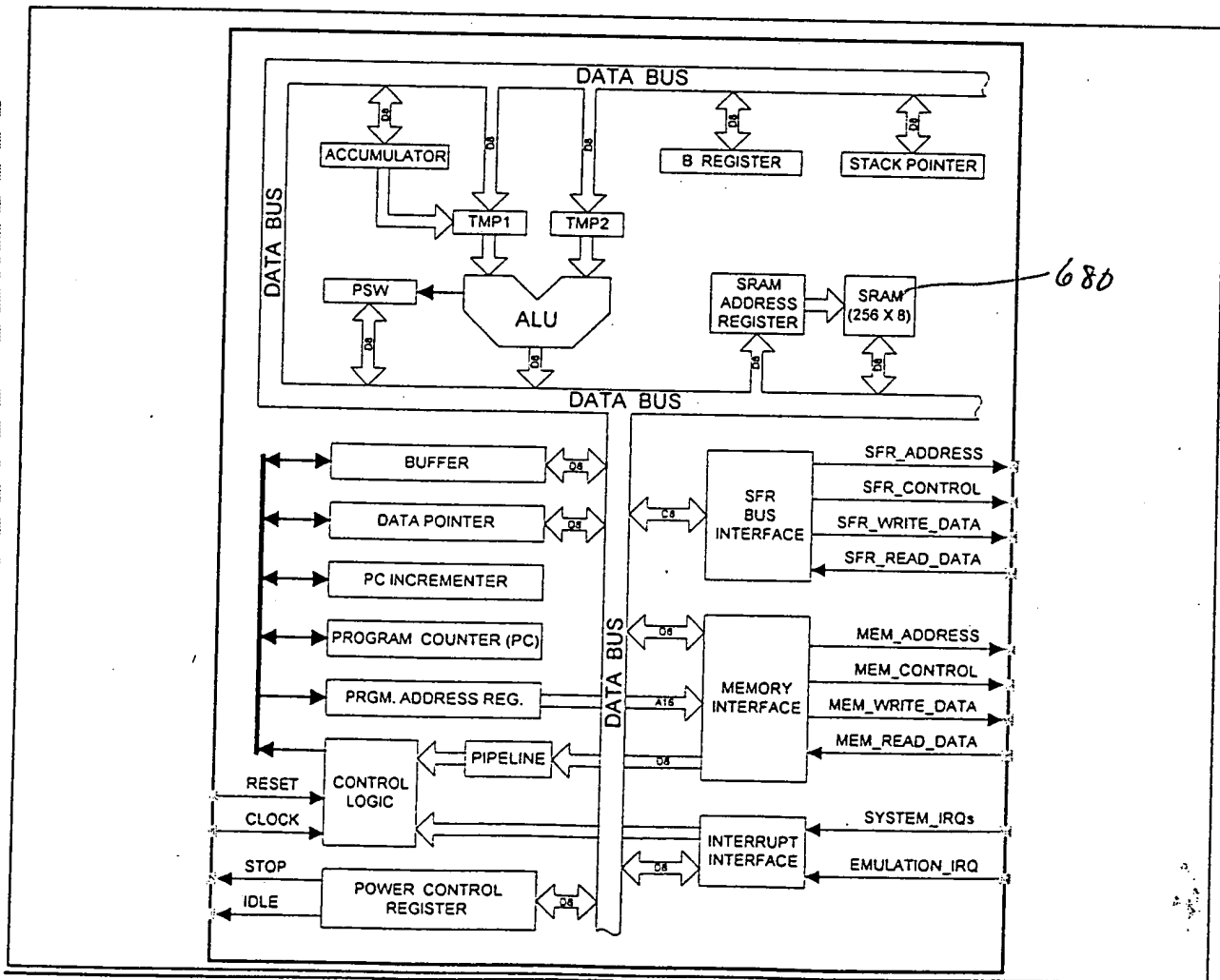


Figure 22. Memory Map

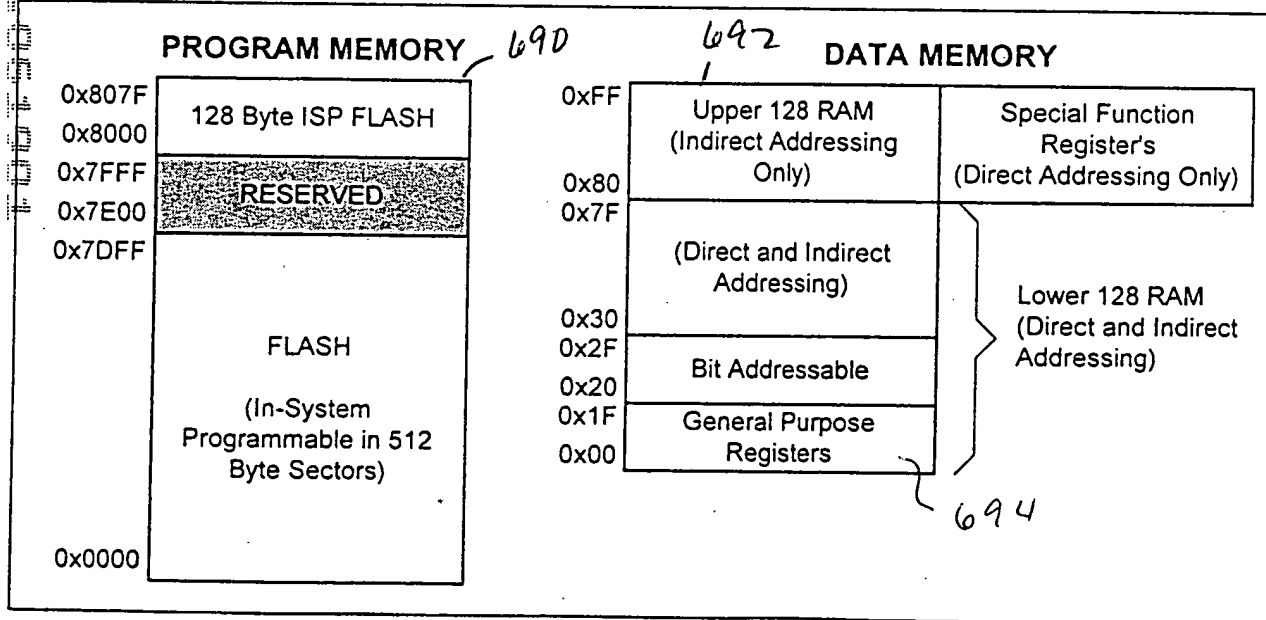
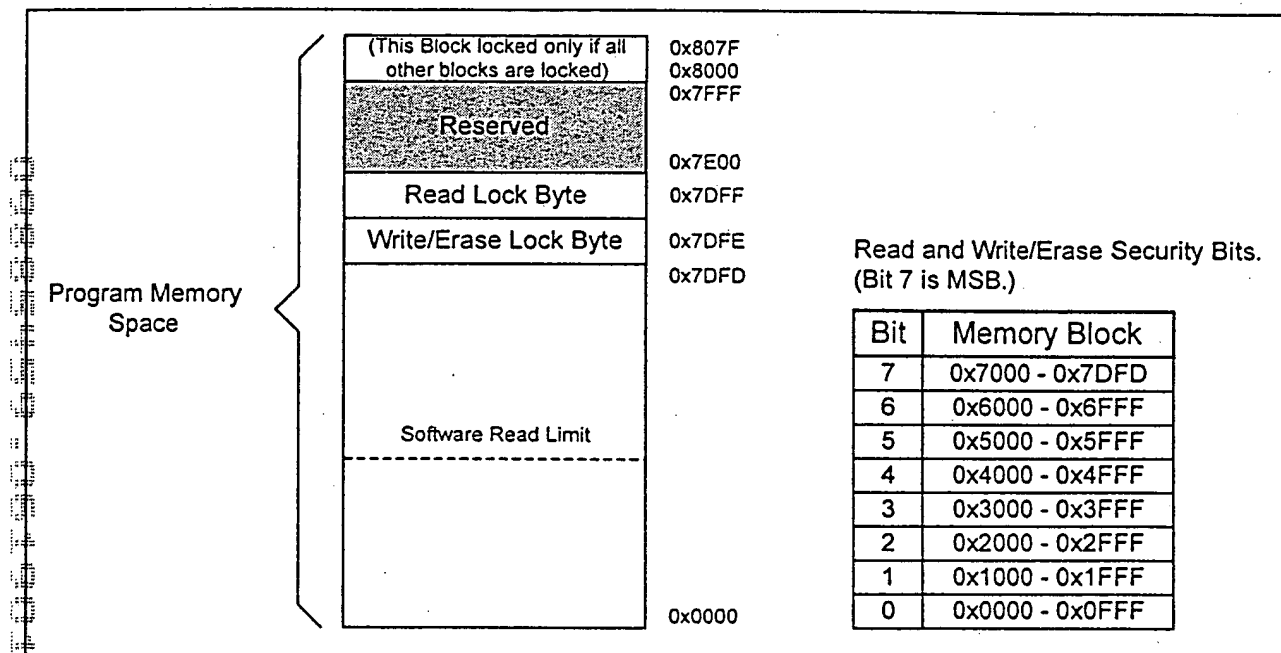


FIGURE 21

Figure 10.1. Flash Program Memory Security Bytes

**FLASH Read Lock Byte**

Bits7-0: Each bit locks a corresponding block of memory. (Bit 7 is MSB.)

0: Read operations are locked (disabled) for corresponding block across the JTAG interface.

1: Read operations are unlocked (enabled) for corresponding block across the JTAG interface.

**FLASH Write/Erase Lock Byte**

Bits7-0: Each bit locks a corresponding block of memory.

0: Write/Erase operations are locked (disabled) for corresponding block across the JTAG interface.

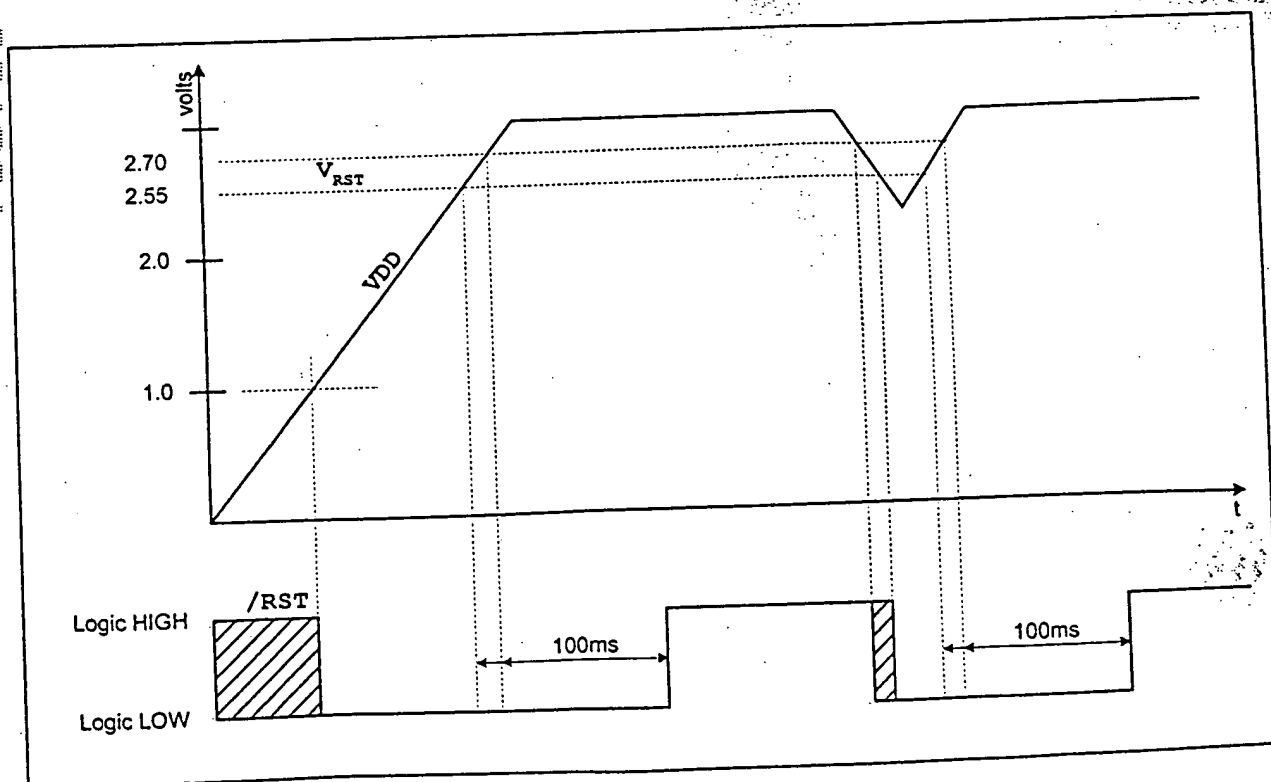
1: Write/Erase operations are unlocked (enabled) for corresponding block across the JTAG interface.

**FLASH Access Limit Register (FLACL)**

The content of this register is used as the high byte of the 16-bit software read limit address. The 16-bit read limit address value is calculated as 0xNN00 where NN is replaced by content of this register on reset. Software running at or above this address is prohibited from using the MOVX and MOVC instructions to read, write, or erase, locations below this address. Any attempts to read locations below this limit will return the value 0x00.

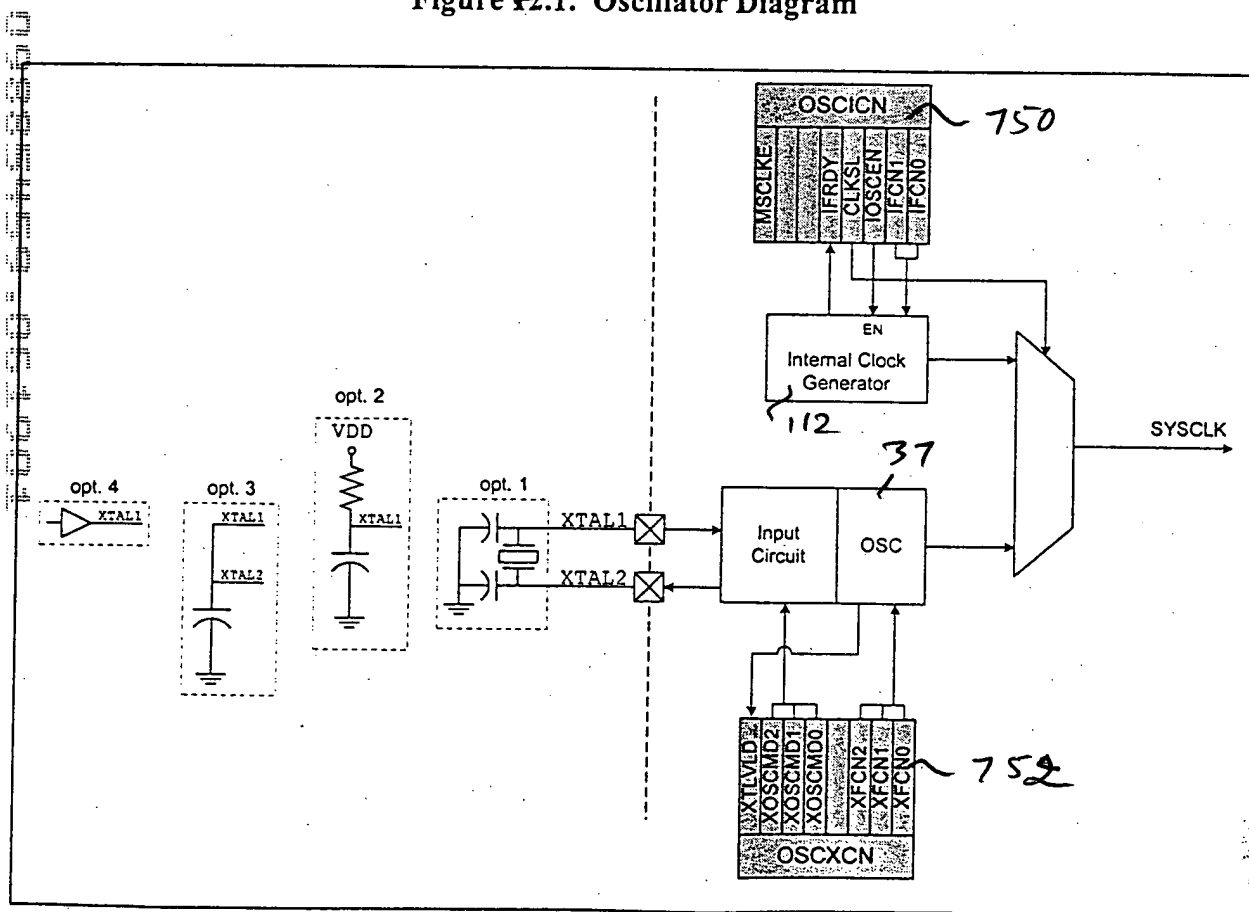
22  
26

Figure 11.2. VDD Monitor Timing Diagram



23  
21

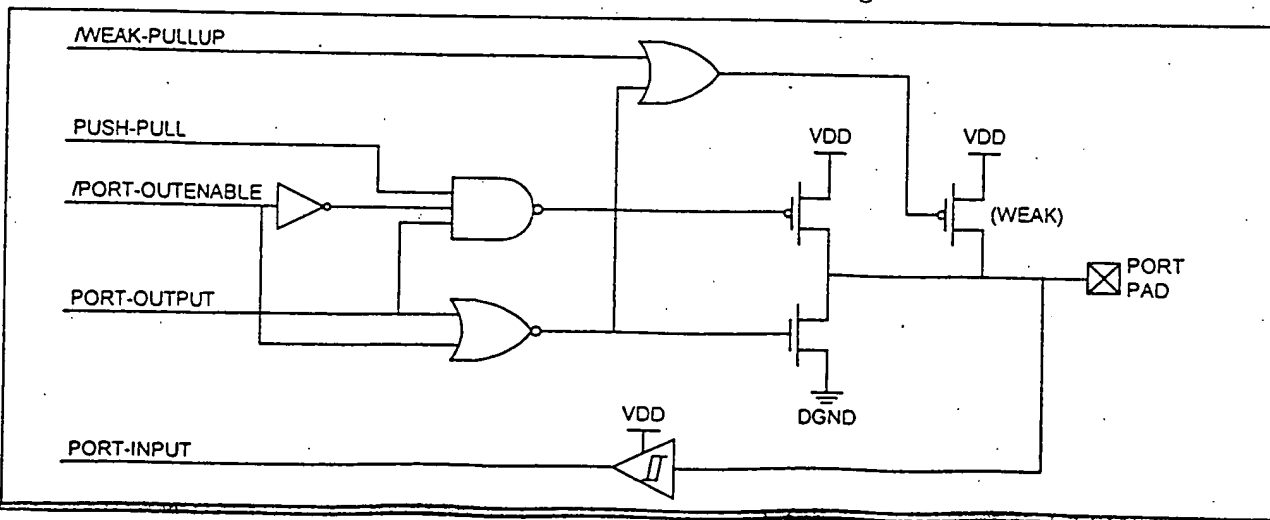
Figure 12.1. Oscillator Diagram



2004-05-20 10:50:00

3924

Figure 13.2. Port I/O Cell Block Diagram







22

The diagram illustrates an I2C bus configuration. It features two horizontal lines representing the SDA (Serial Data) and SCL (Serial Clock) lines. A pull-up resistor, labeled '784' with an arrow, is connected to the SDA line and a 5V VDD supply. Three devices are connected to the bus: a Master Device and two Slave Devices (Slave Device 1 and Slave Device 2). The Master Device and Slave Device 1 are connected to a 3V VDD supply, while Slave Device 2 is connected to a 5V VDD supply. Each device has two pins connected to the SDA and SCL lines.

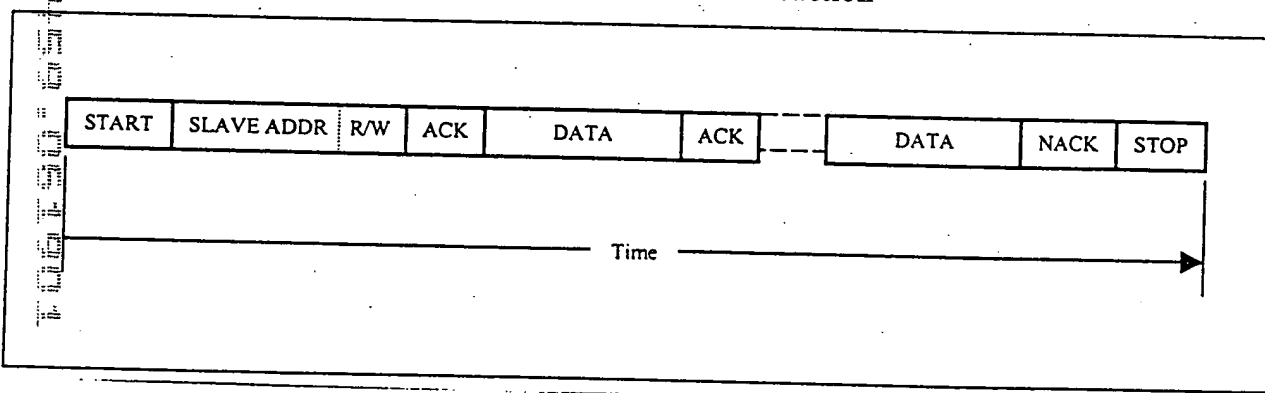
780

[illegible]

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~~19~~

Figure 14.3. SMBus Transaction

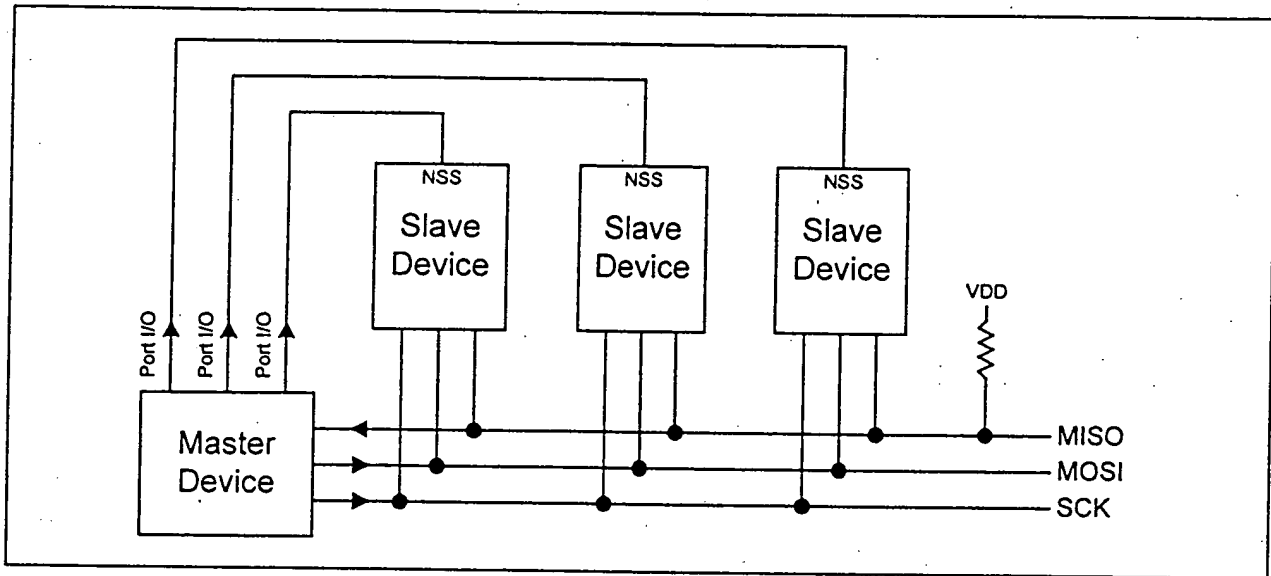


e y



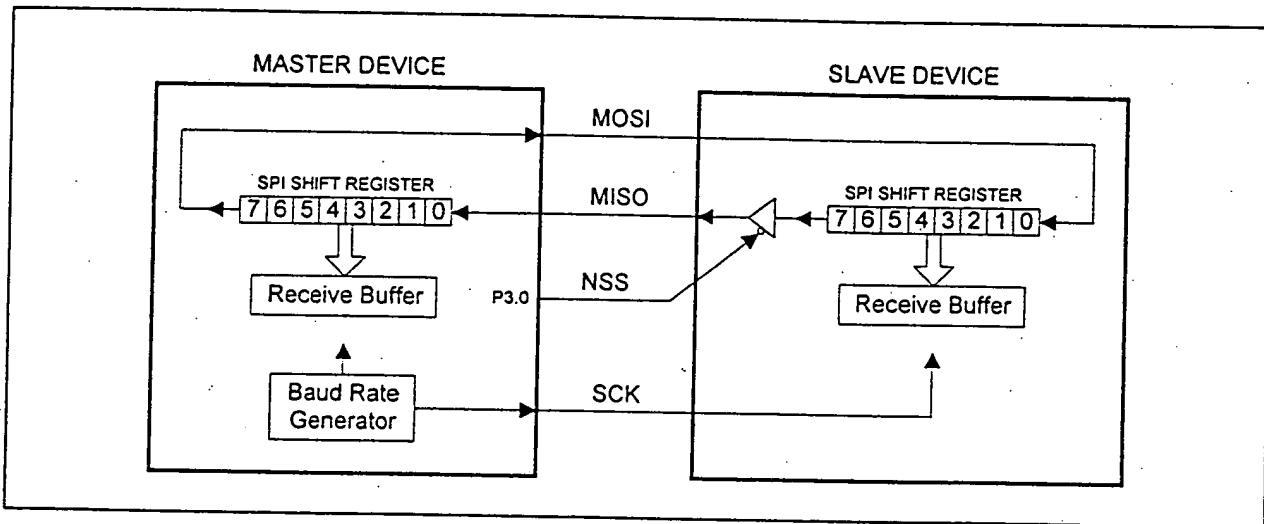
30 29

Figure 15.2. Typical SPI Interconnection



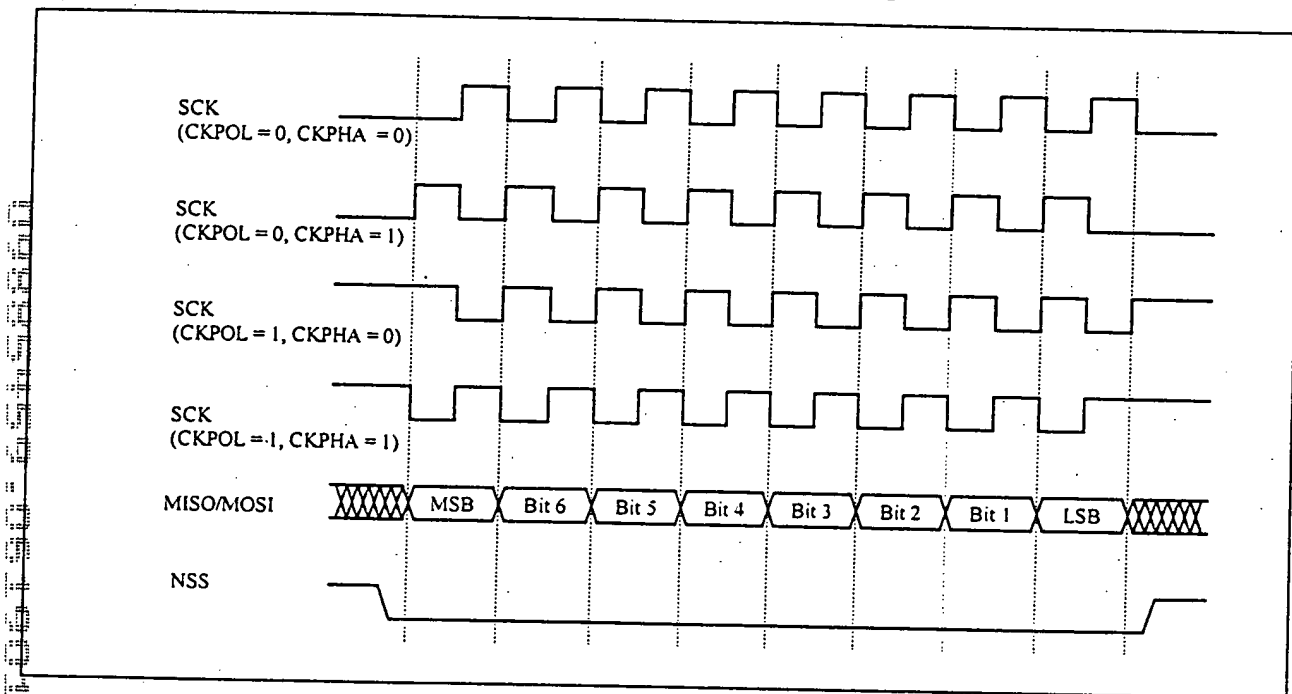
30  
30

Figure 15.3. Full Duplex Operation



31  
~~32~~  
40

Figure 15.4. Data/Clock Timing Diagram



820

FIG 32

Figure 10.1. UAK1 BLOCK Diagram

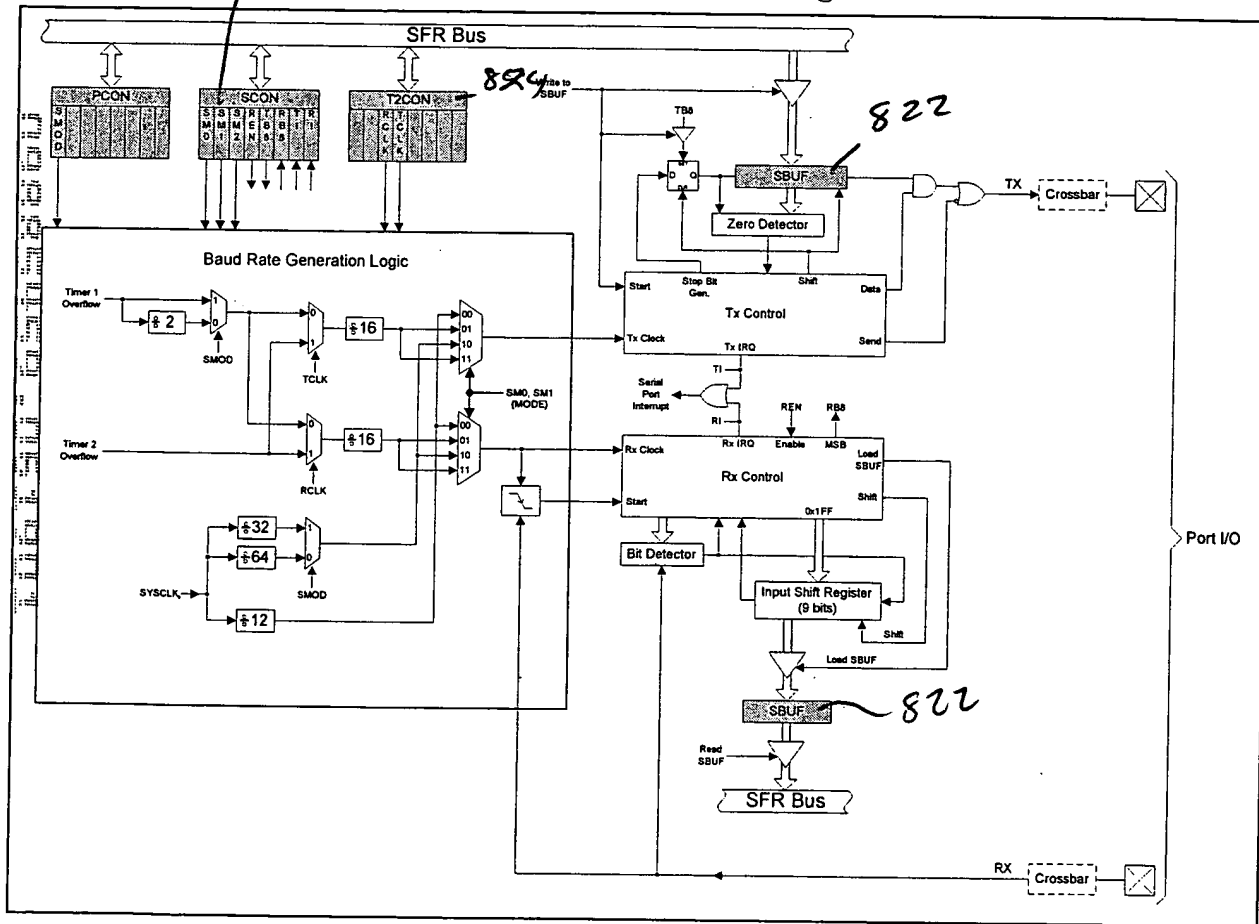




Figure 16.2. UART Mode 0 Interconnect

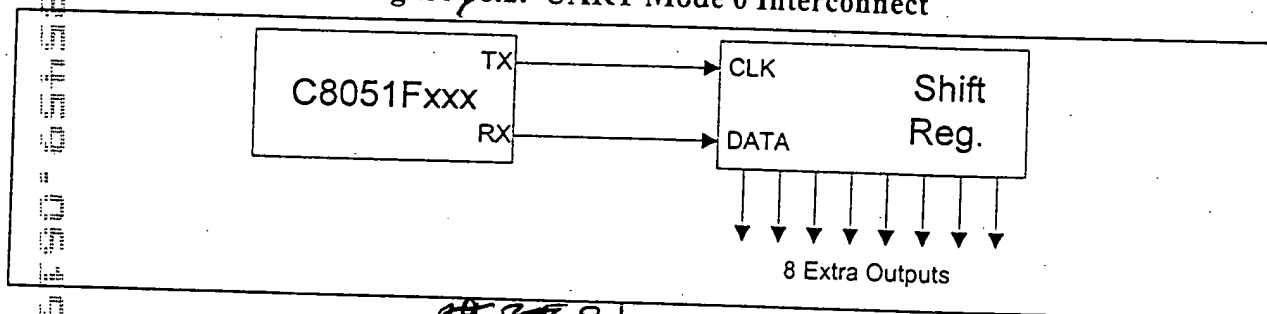
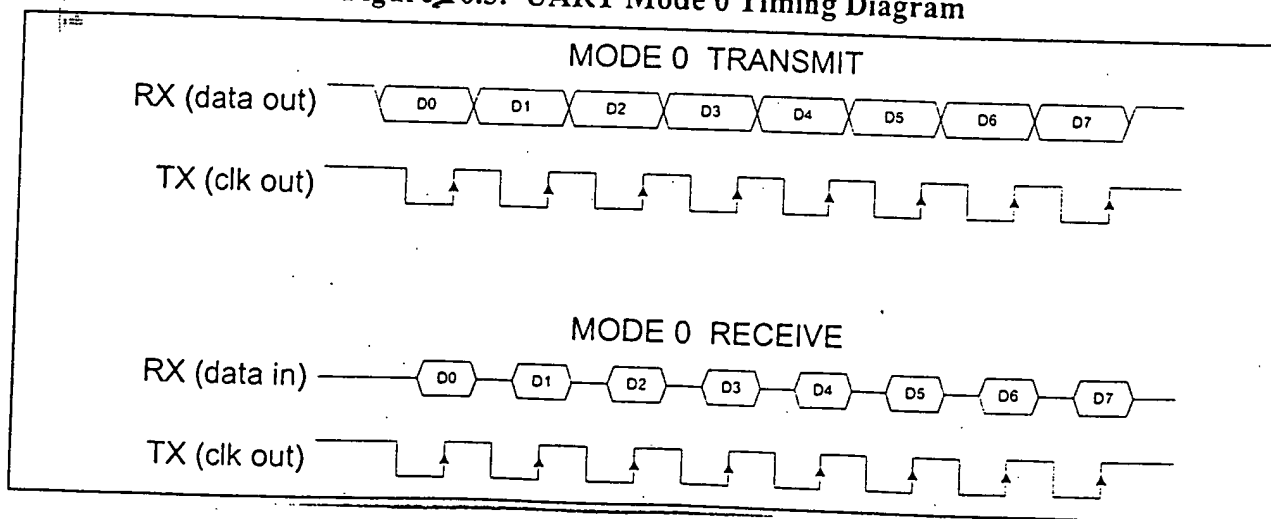
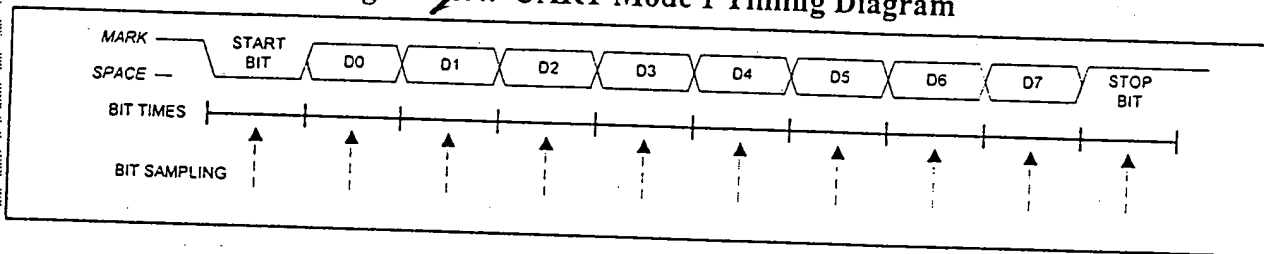


Figure 16.3. UART Mode 0 Timing Diagram



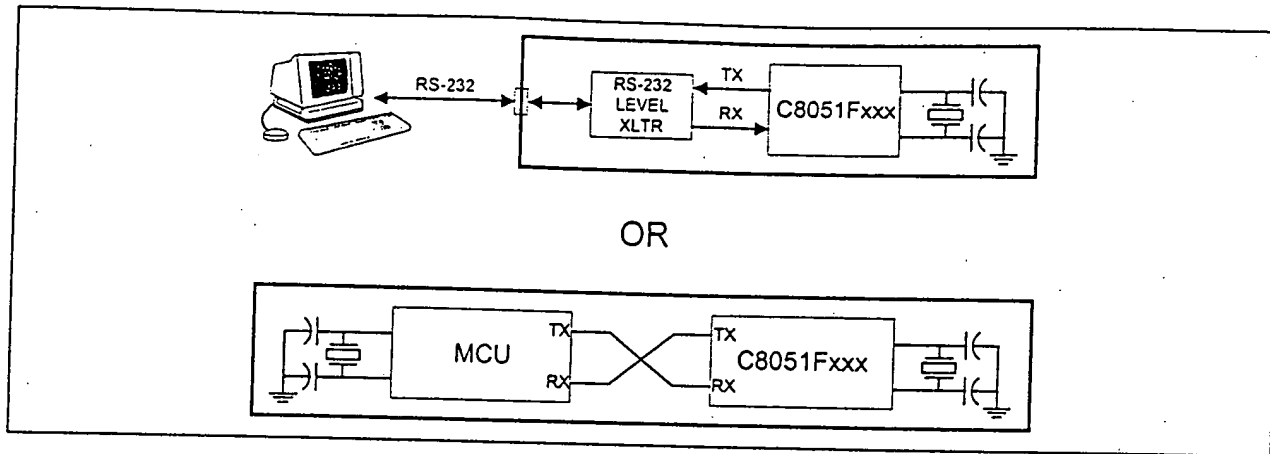
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**Figure 16.4. UART Mode 1 Timing Diagram**



36  
41

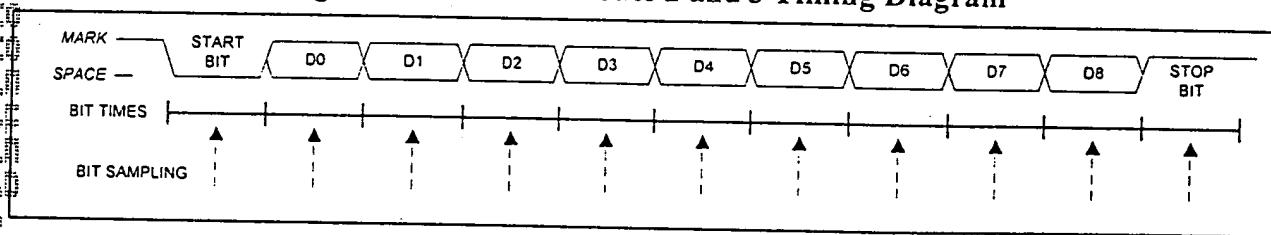
Figure 16.5. UART Modes 1, 2, and 3 Interconnect Diagram



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38  
42

Figure 18.6. UART Modes 2 and 3 Timing Diagram



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38  
49

Figure 16.7. UART Multi-Processor Mode Interconnect Diagram

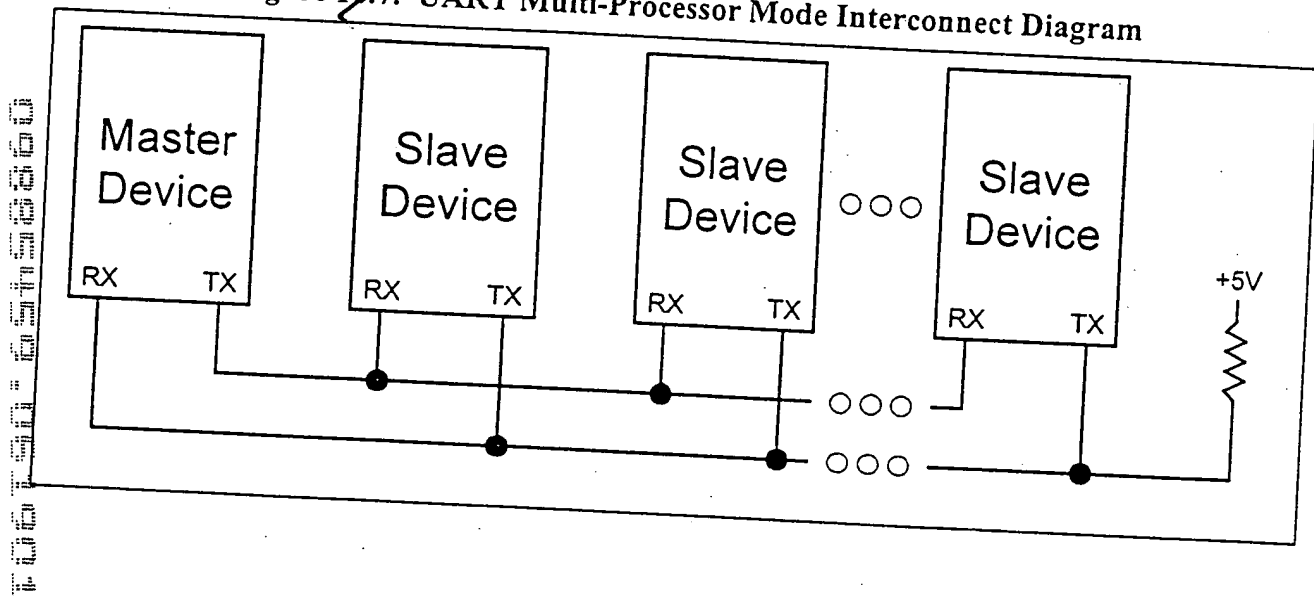
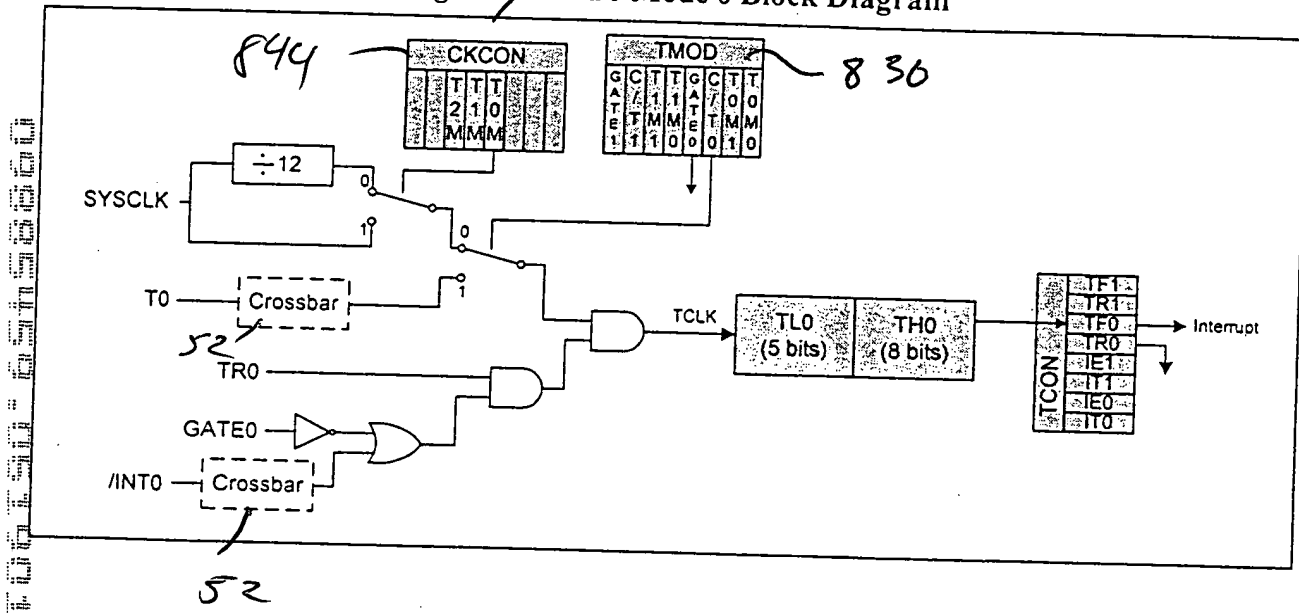


Figure 17.1. T0 Mode 0 Block Diagram



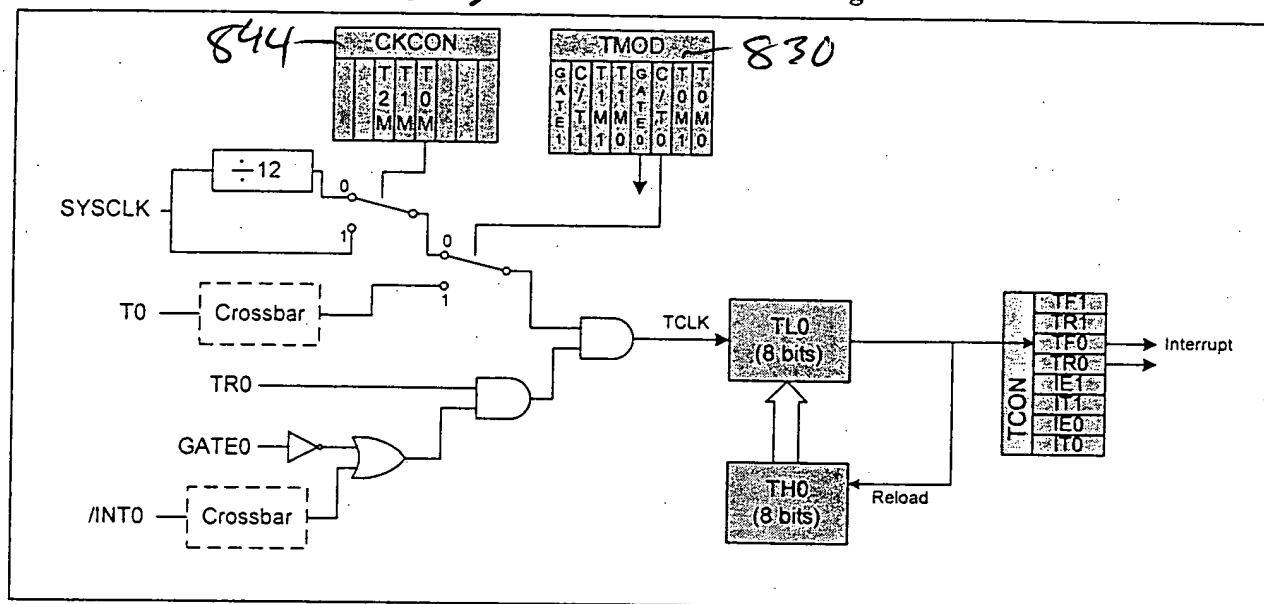
40  
~~45~~

844

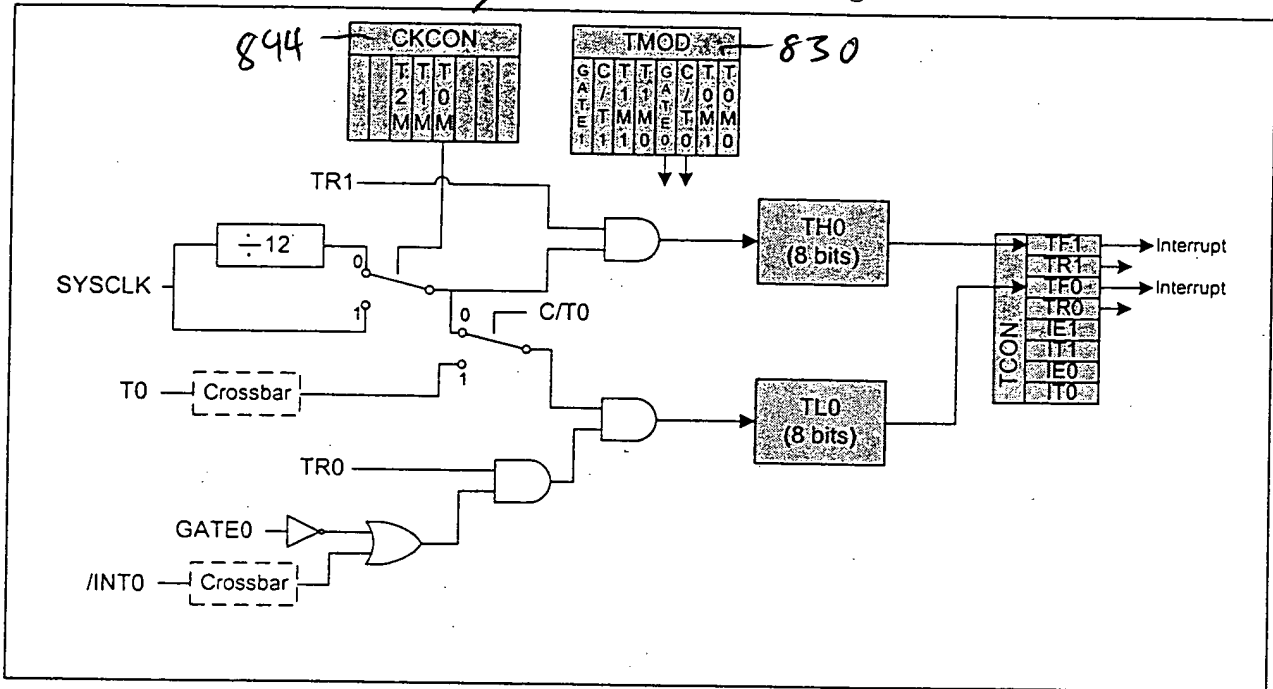
CKCON					
1	2	3	4	5	6
T1	T2	T1	T0	T1	T0
M	M	M	M	M	M

830

TMOD					
1	2	3	4	5	6
GATE	C/T	T1	T0	GATE	T1
1	1	M	M	0	0

[illegible]

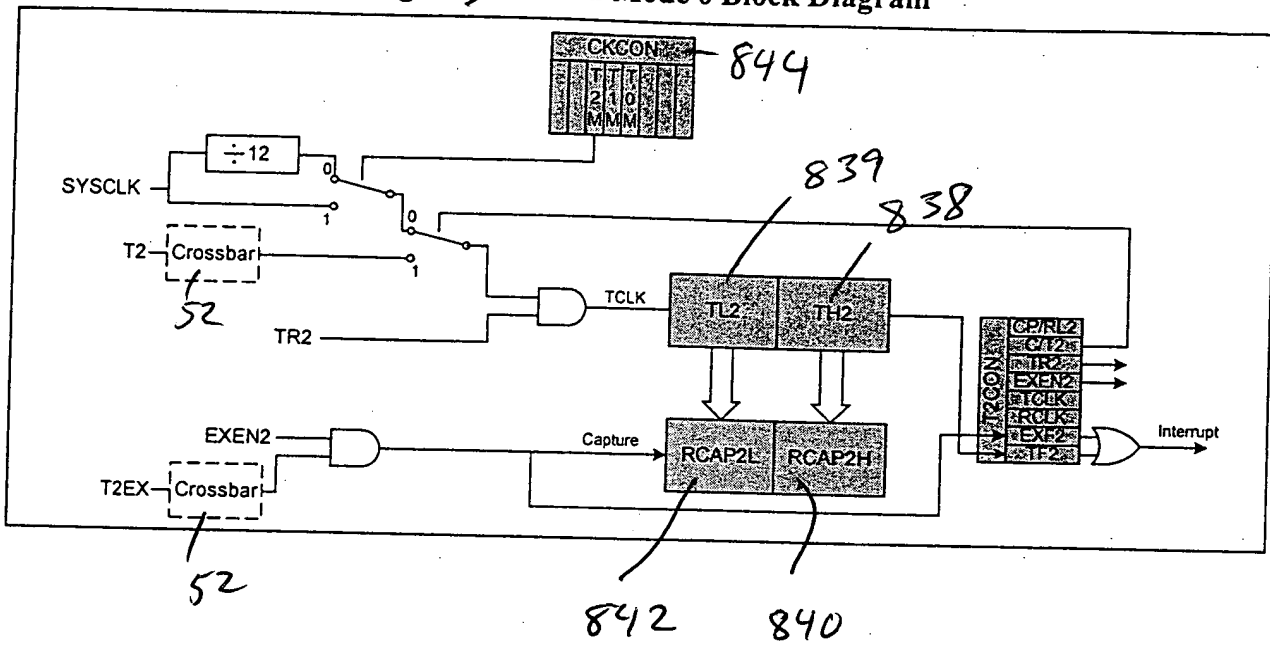
41  
46  
Figure 17.3. T0 Mode 3 Block Diagram



00000000000000000000000000000000



Figure 17.11. T2 Mode 0 Block Diagram



43  
43  
Figure 17.12. T2 Mode 1 Block Diagram

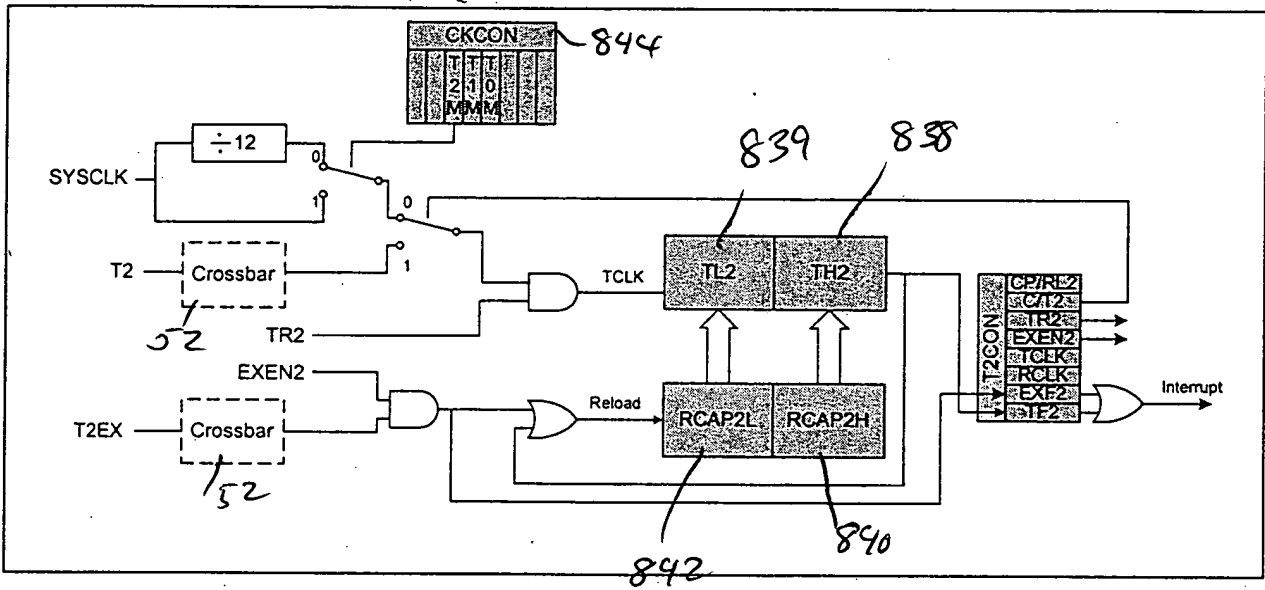
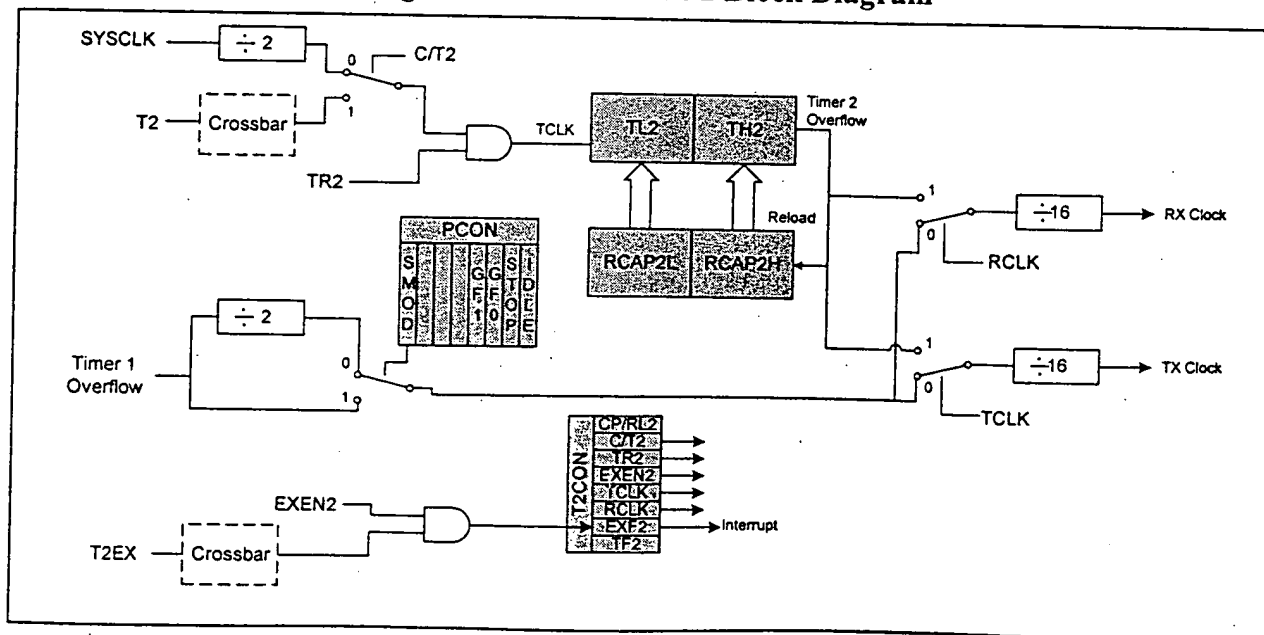
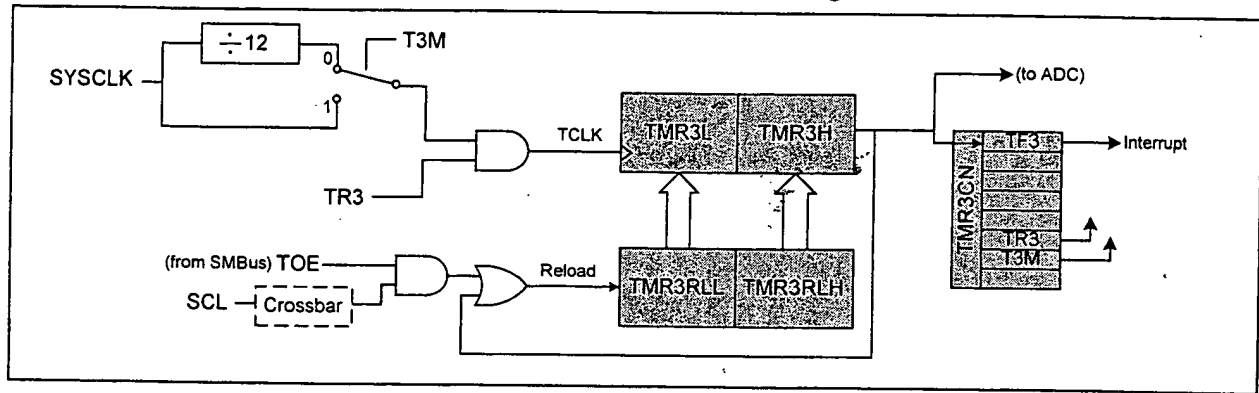


Figure 17.13. T2 Mode 2 Block Diagram



45  
Figure 17-19. Timer 3 Block Diagram

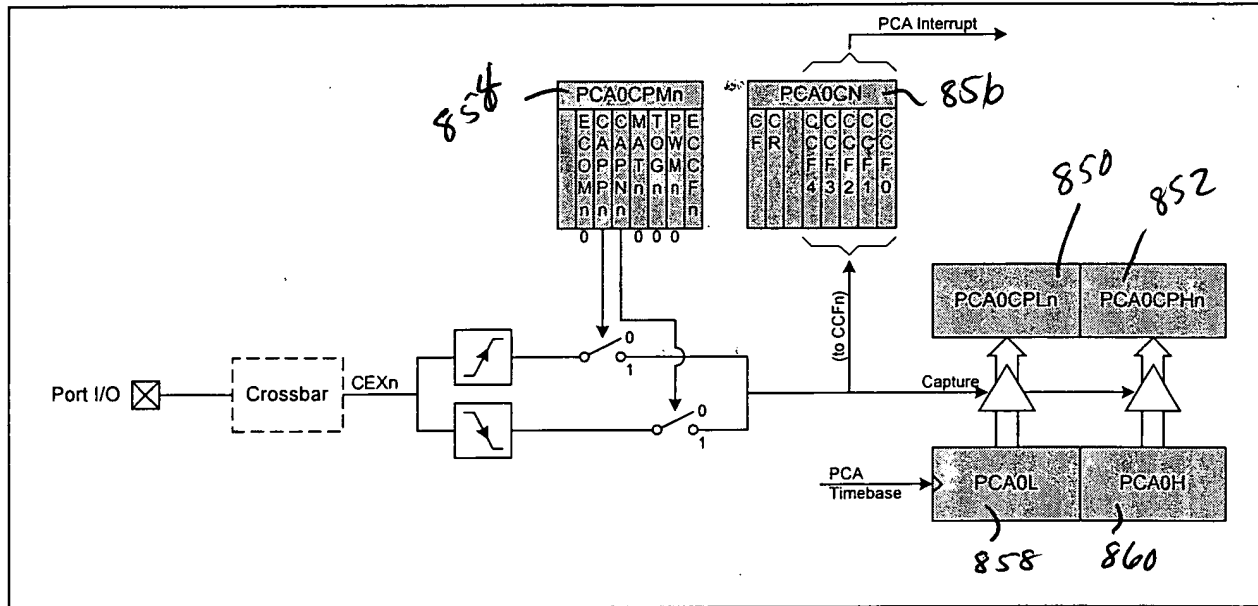


100T30-65H3330



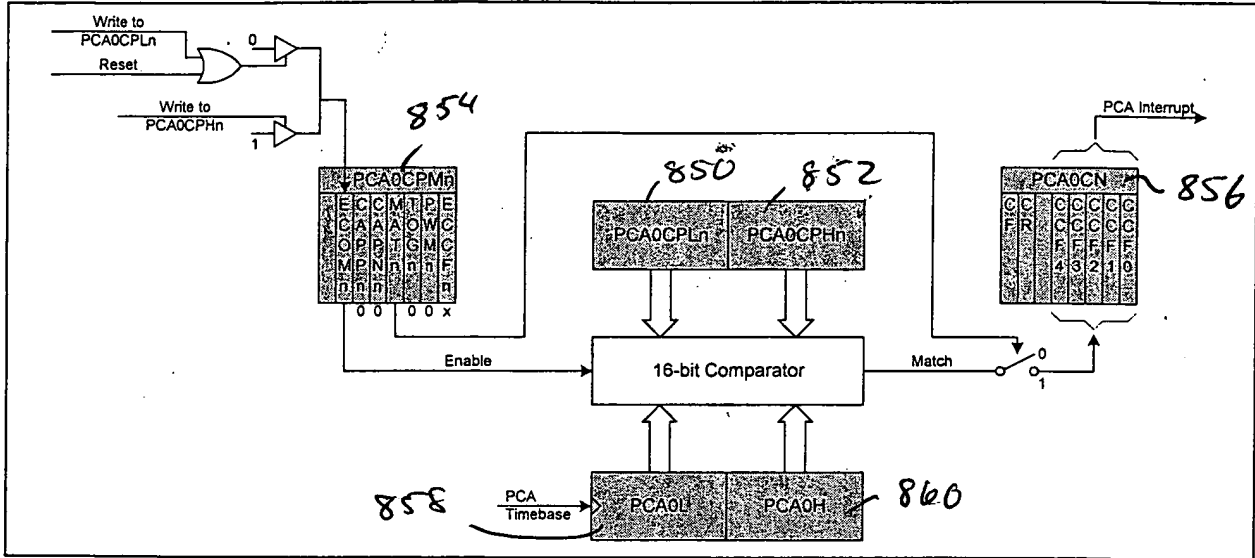
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Figure 18.3. PCA Capture Mode Diagram



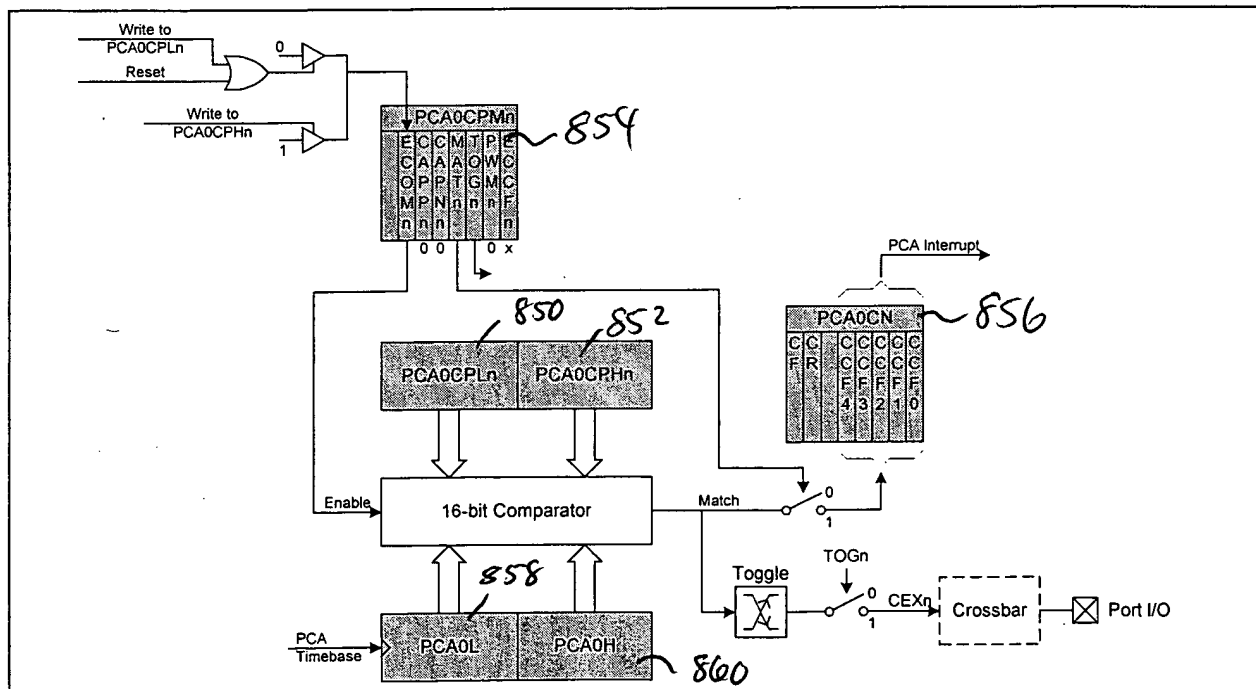
48

Figure 18.4. PCA Software Timer Mode Diagram



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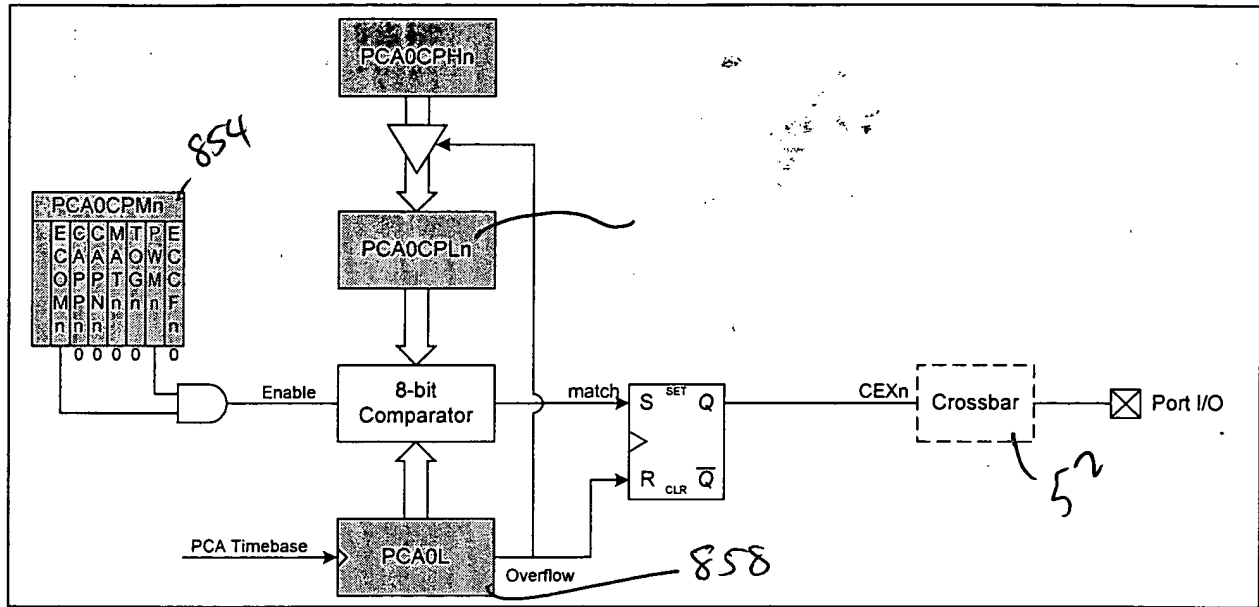
49  
50  
Figure 18.5. PCA High Speed Output Mode Diagram





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50  
Figure 186. PCA PWM Mode Diagram



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Figure 18.7. PCA Counter/Timer Block Diagram

